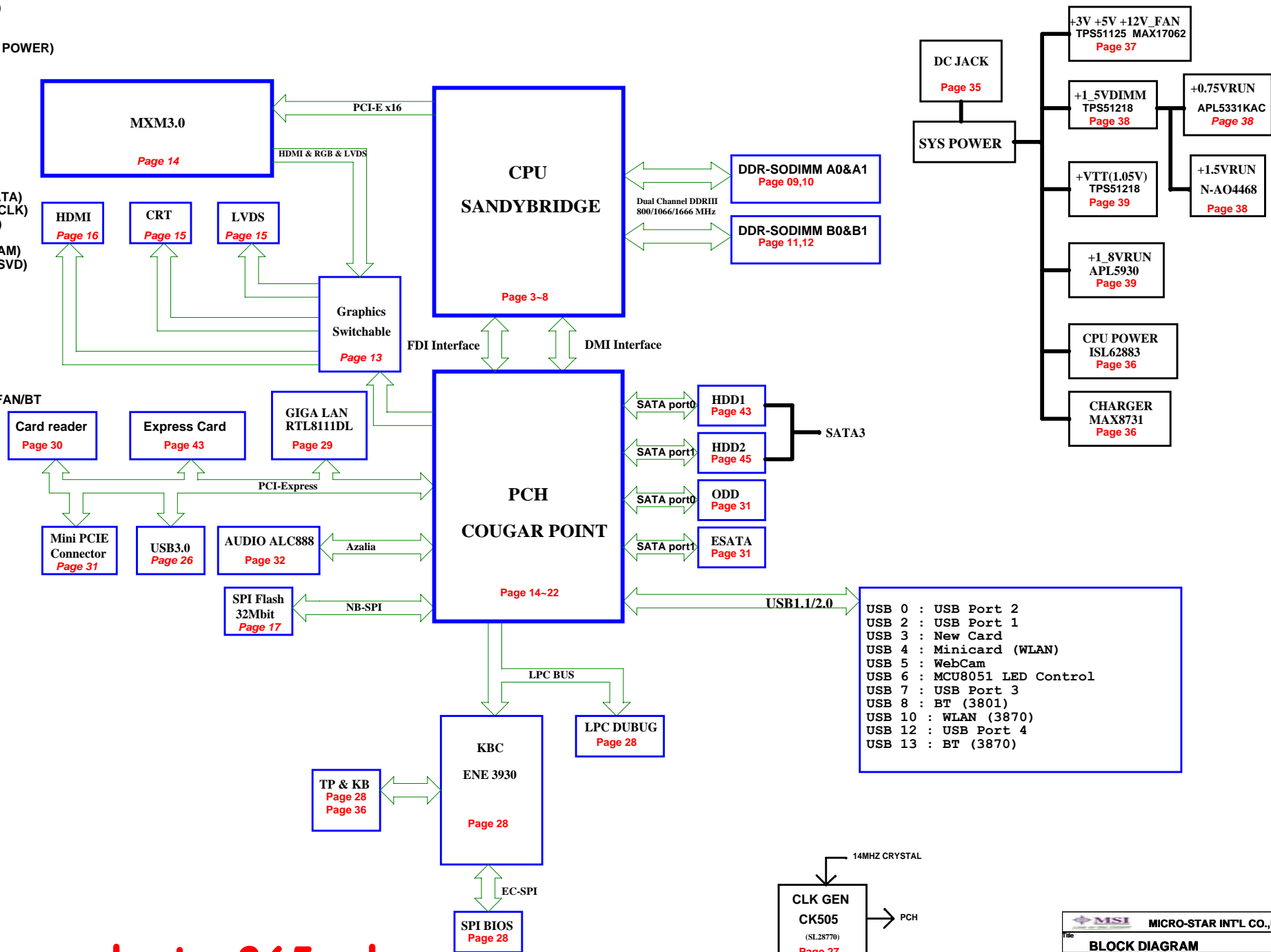


Huron River Platform

- 01 : BLOCK DIAGRAM
 02 : PLATFORM
 03 : PROCESSOR-1 (HOST BUS)
 04 : PROCESSOR-2 (DDR3)
 05 : PROCESSOR-3 (POWER)
 06 : PROCESSOR-4 (GRAPHICS POWER)
 07 : PROCESSOR-5 (GND)
 08 : PROCESSOR-6 (RESERVE)
 09 : DDR3 SODIMM A0
 10 : DDR3 SODIMM A1
 11 : DDR3 SODIMM B0
 12 : DDR3 SODIMM B1
 13 : SWITCH
 14 : MXM3.0 Slot
 15 : CRT/LVDS/CCD
 16 : HDMI
 17 : CougarPoint (HDA/JTAG/SATA)
 18 : CougarPoint (PCI-E/SMBUS/CLK)
 19 : CougarPoint (DMI/FDI/GPIO)
 20 : CougarPoint (LVDS/DDI)
 21 : CougarPoint (PCI/USB/NVRAM)
 22 : CougarPoint (GPIO/NCTF/RSVD)
 23 : CougarPoint (POWER)
 24 : CougarPoint (POWER)
 25 : CougarPoint (GND)
 26 : USB3.0
 27 : CLOCK GEN (SL28770)
 28 : KBC/EC/uP (KB3930)
 29 : GIGA LAN (RTL8111DL)
 30 : Card Reader (UB6250)
 31 : WLAN/TP/BT/USB
 32 : HDD2/ODD/ESATA Combo/FAN/BT
 33 : AUDIO(ALC888)
 34 : LED_8051
 35 : M_Battery select
 36 : M_Battery Charger
 37 : M_System Power
 38 : M_DIMM_1.5VRUN
 39 : M_VTT_1.8VRUN
 40 : M_CPU Power
 41 : M_0.8V
 42 : EMI/Screw
 43 : 16F1A_NewCard/HDD1
 44 : 16F1B_IO/Audio Board
 45 : 16F1C_HDD2
 46 : 16F1D_Cap Sensor Board
 47 : 16F1E_Touch Pad L/R Key
 48 : 16F1F_CDLED_RF
 49 : 16F1G_ABLED Front
 50 : 16F1H_ABLED_L
 51 : 16F1I_ABLED_R
 52 : 16F1J_CDLED_L
 53 : 16F1K_CDLED_LF
 54 : PowerDown Sequence
 55 : PowerOn Sequence
 56 : History



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

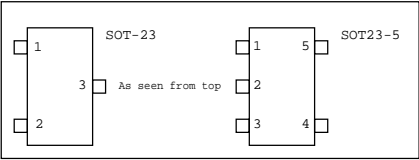
Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	12V	S0, (S3-S5)	
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0, S3	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VRUN_CK505	3.3V	S0	Clock, MCH
+3VSUS	3.3V	S0, S3	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0, (S3-S4)	DDR core
+1_5VSUS	1.5V	S0	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDR command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	GMCH Graphics core rail

Net Naming Conventions

Suffix
= Active Low Signal

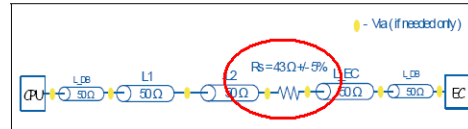
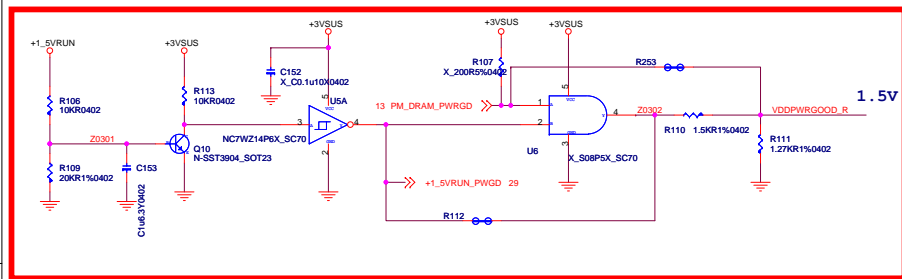
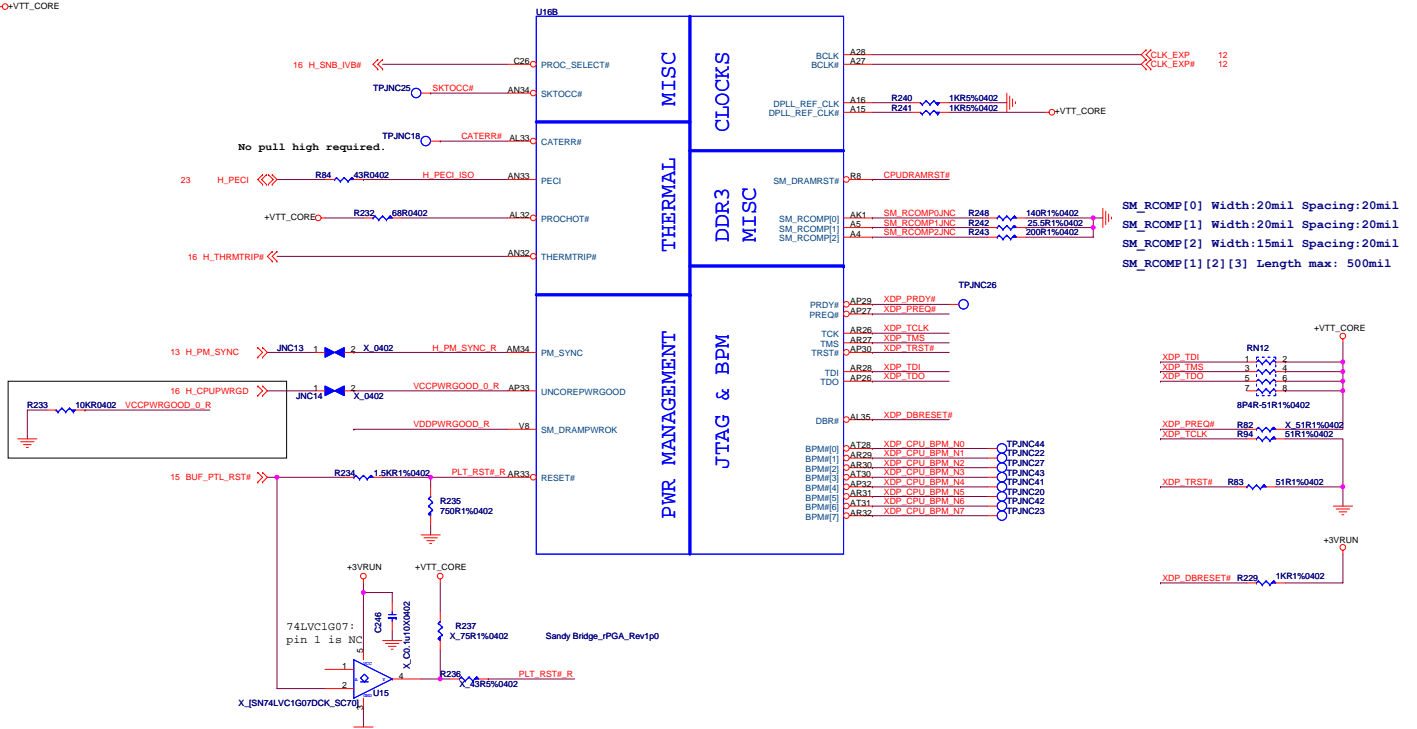
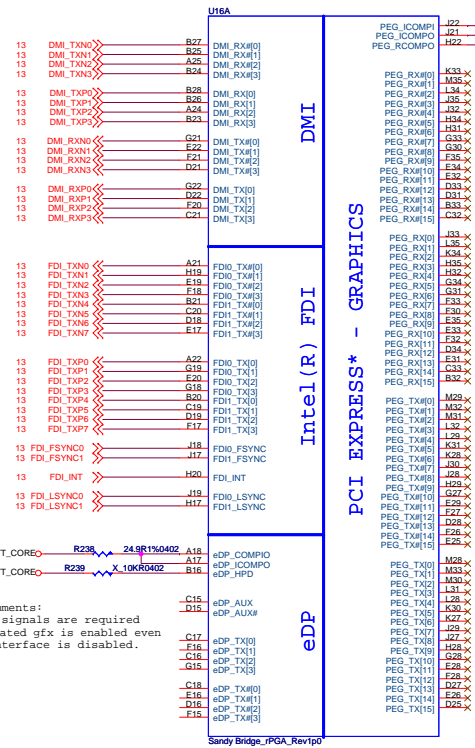
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



Power States	SLP S3#	SLP S4#	SLP S5#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

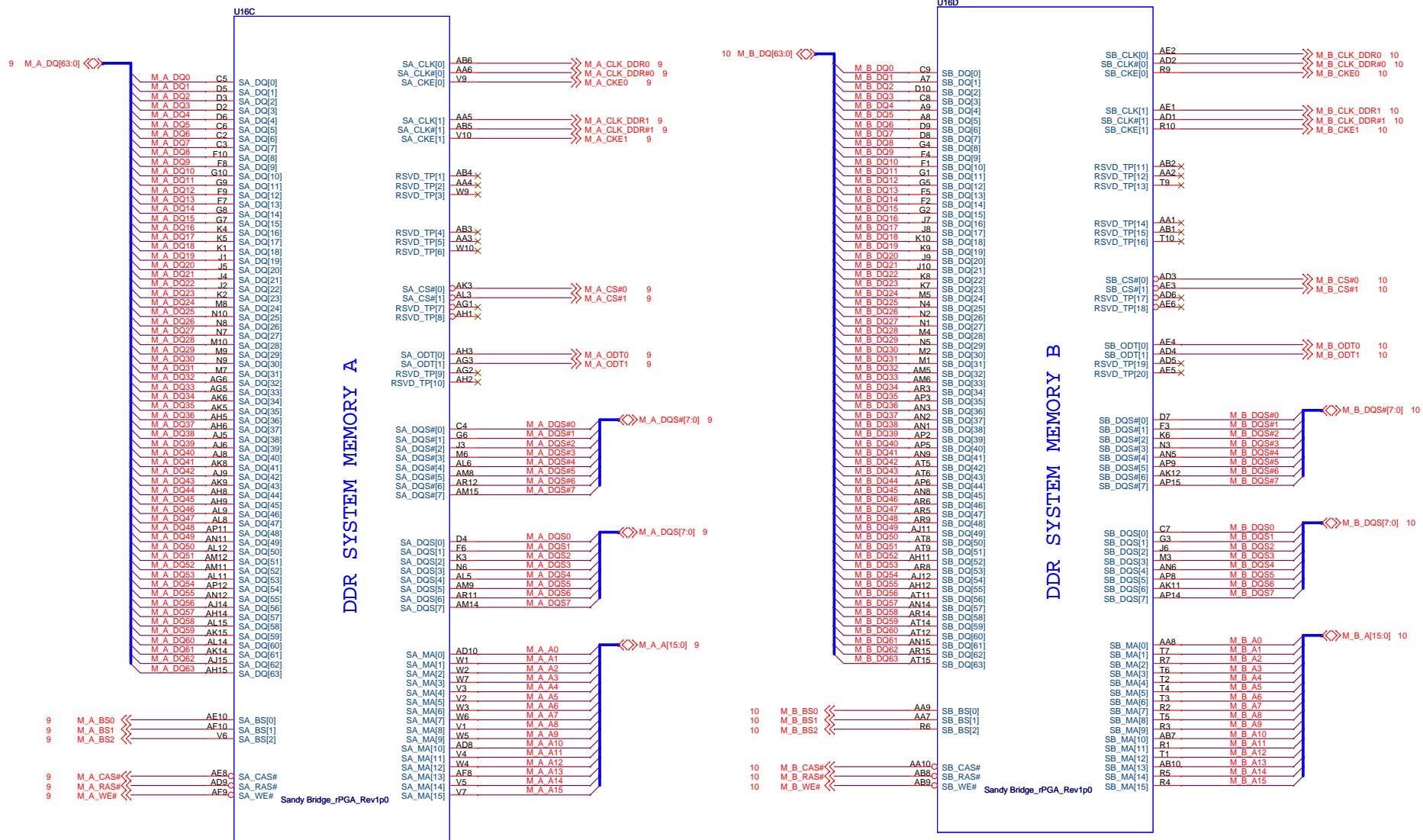
SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)

[illegible]

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Title				
PROCESSOR				
Size	Document Number			Rev
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Date:	Wednesday, September 29, 2010	Sheet	3	of 42

SANDYBRIDGE PROCESSOR (DDR3)



SANDYBRIDGE PROCESSOR (POWER)

Vcc for Processor core 0.3-1.1V

Iccmax: SV-QC 94A;
Iccmax: SV-DC 53A;

Icc_TDC: SV-DC 55A;
Icc_TDC: SV-DC 38A;

U16F

POWER

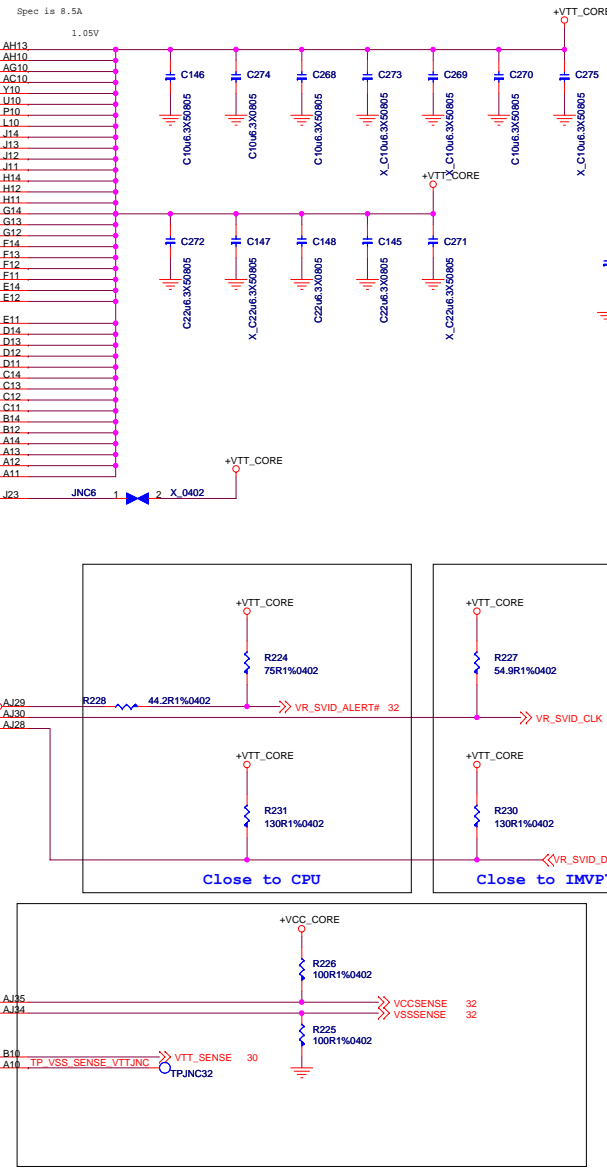
- AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
Y25 VCC61
Y24 VCC62
Y23 VCC63
Y22 VCC64
Y21 VCC65
Y20 VCC66
Y19 VCC67
Y18 VCC68
Y17 VCC69
Y16 VCC70
Y15 VCC71
Y14 VCC72
Y13 VCC73
Y12 VCC74
Y11 VCC75
Y10 VCC76
Y09 VCC77
Y08 VCC78
Y07 VCC79
Y06 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

PEG AND DDR

CORE SUPPLY

SVID

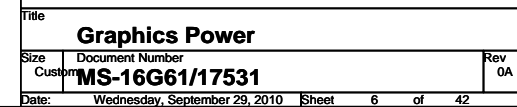
SENSE LINES



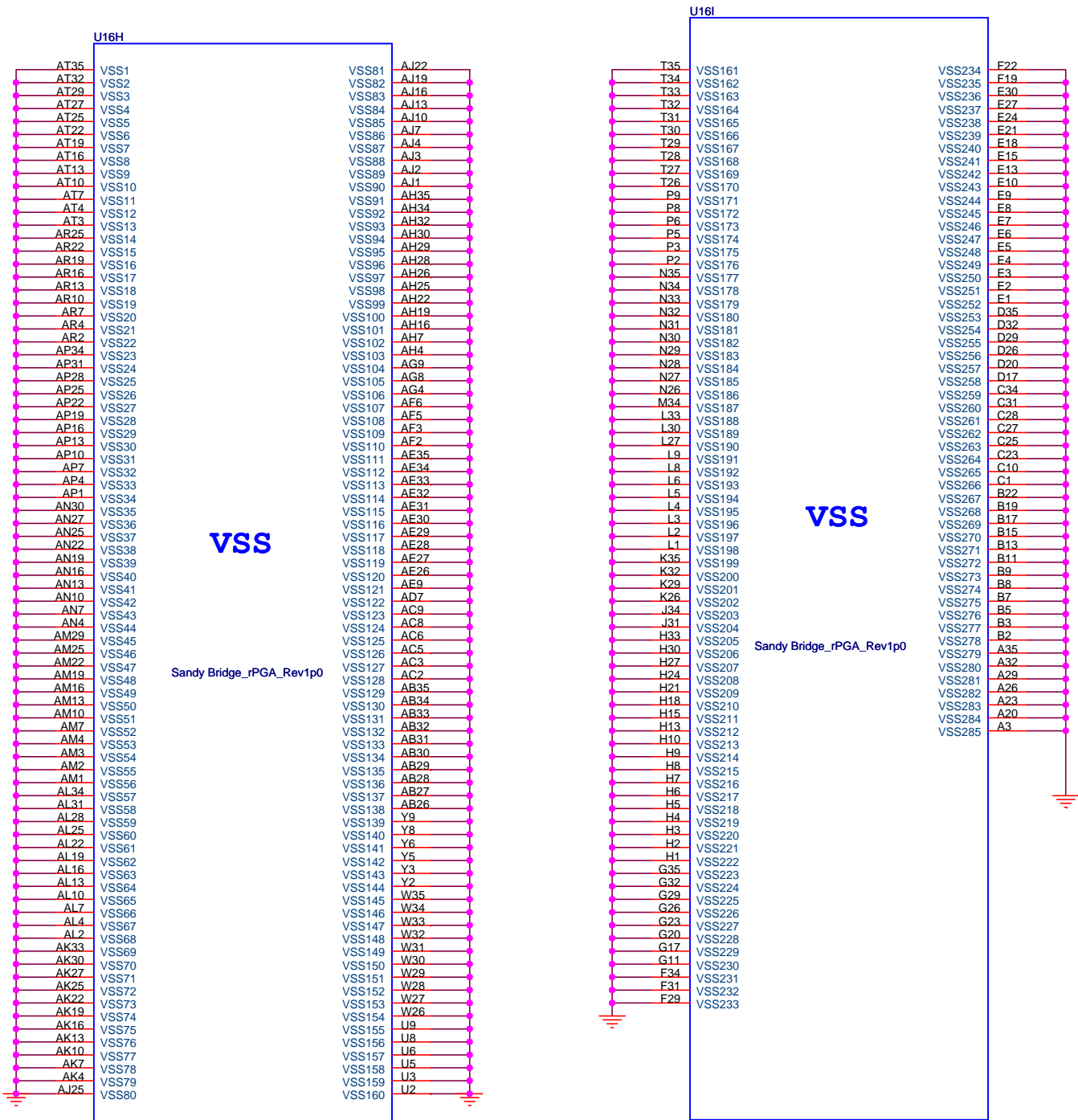
	148X schematic	CRB
+VCC_CORE	10UFx10 22UFx16 330UFx6	10UFx10 22UFx16 470UFx4
+VTT_CORE	10UFx7 22UFx5 330UFx2	22UFx29 330UFx2

Title PROCESSOR POWER		
Size Customer	Document Number MS-16G61/17531	Rev 0A
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SANDYBRIDGE PROCESSOR (GND)

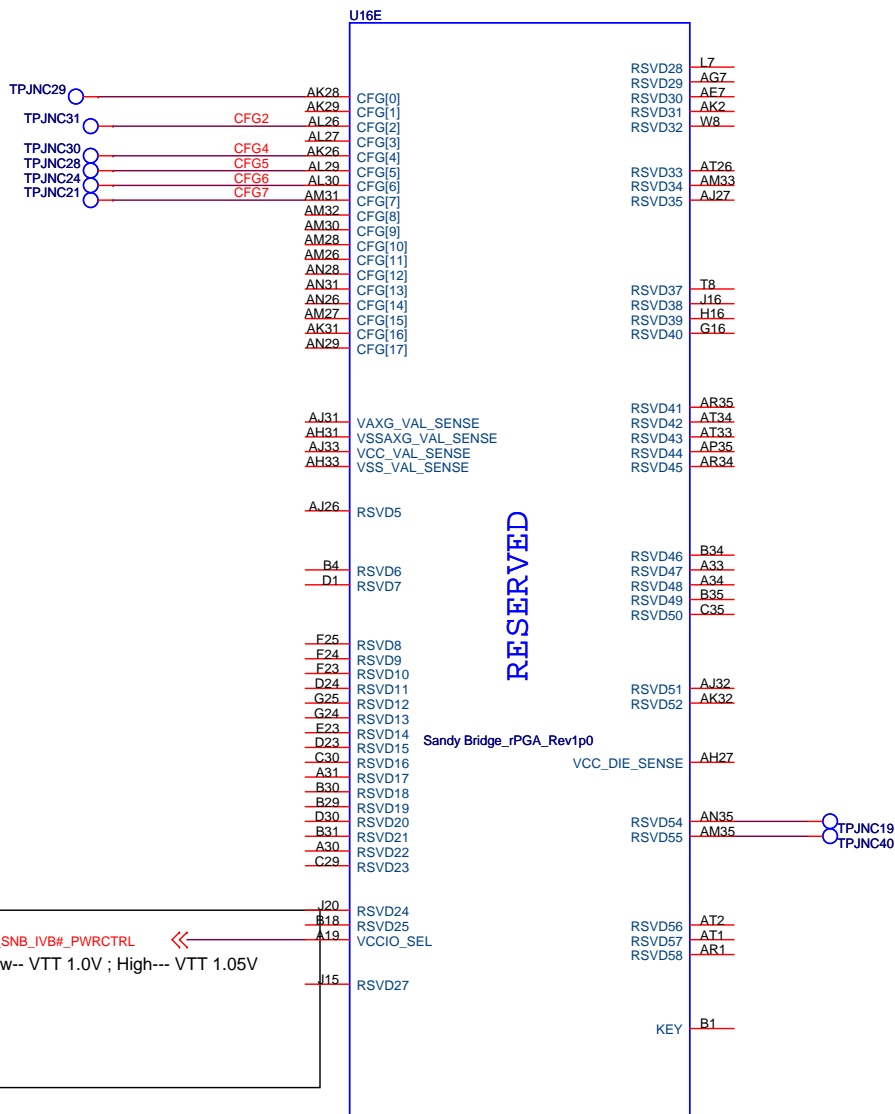


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Title			
PROCESSOR GND			
Size	Document Number		Rev
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SANDYBRIDGE PROCESSOR (RESERVED)

The CFG signals have a default value of "1" if not terminated on the board.



CFG3 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	<p>1:Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0:Enabled; An external Display Port device is connected to the Embedded Display Port</p>

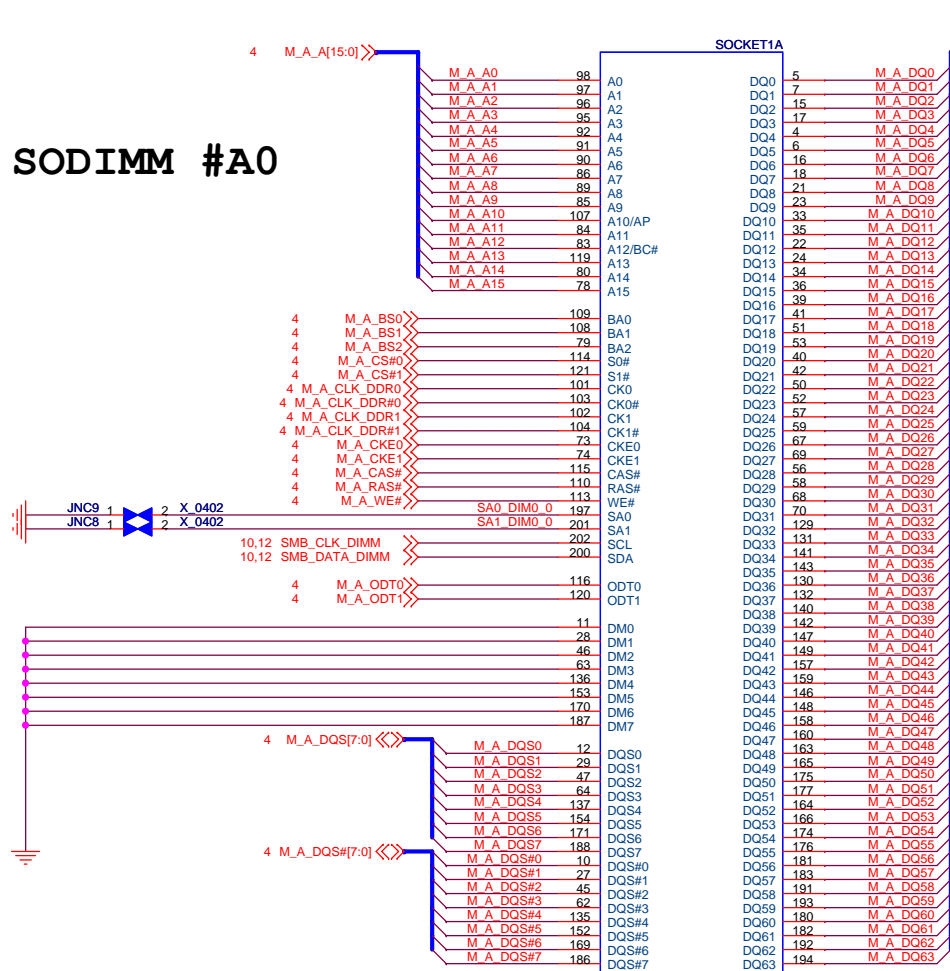
PCI-Express Configuration Select	
CFG[5:6]	<p>11: Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01: Reserved--(device 1 functions 1 disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable</p>

PEG DEFER TRAINING	
CFG7	1 : (Default) PEG train immediately following xxRESETB de assertion 0 : PEG wait for BIOS for training

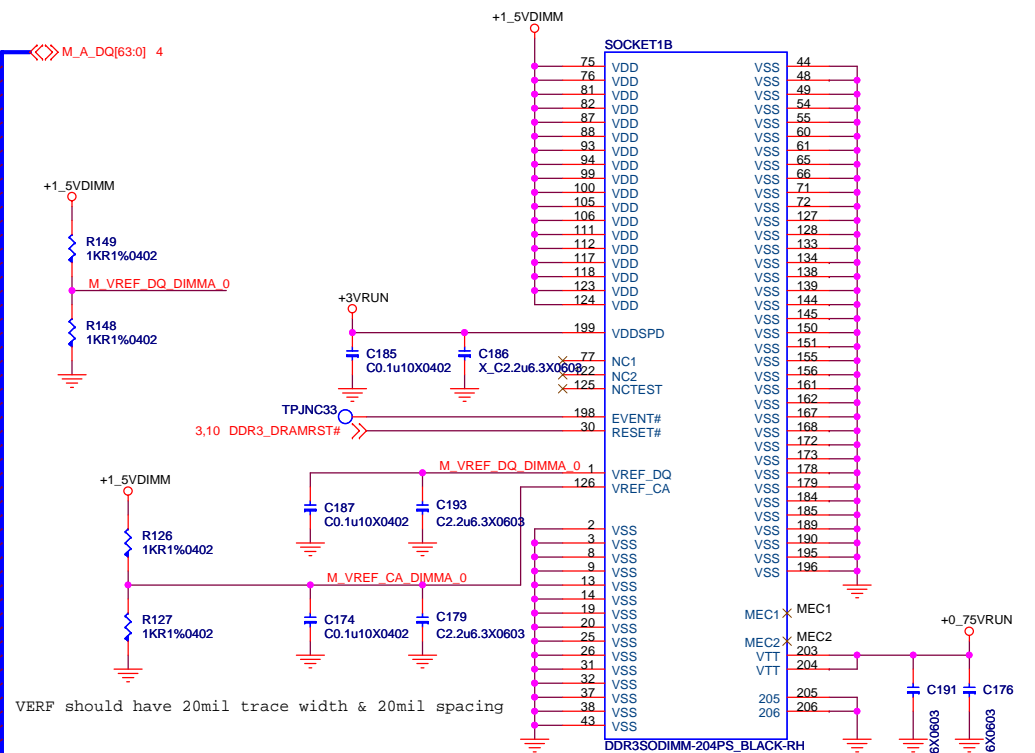
DATASHEET记录	
CFG[17:7]	Reserved configuration lanes. A test point may be placed on the board for these lands.

Title				
PROCESSOR RESERVED				
Size	Document Number			Rev
Custom	MS-16G61/17531			0A
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SODIMM #A0



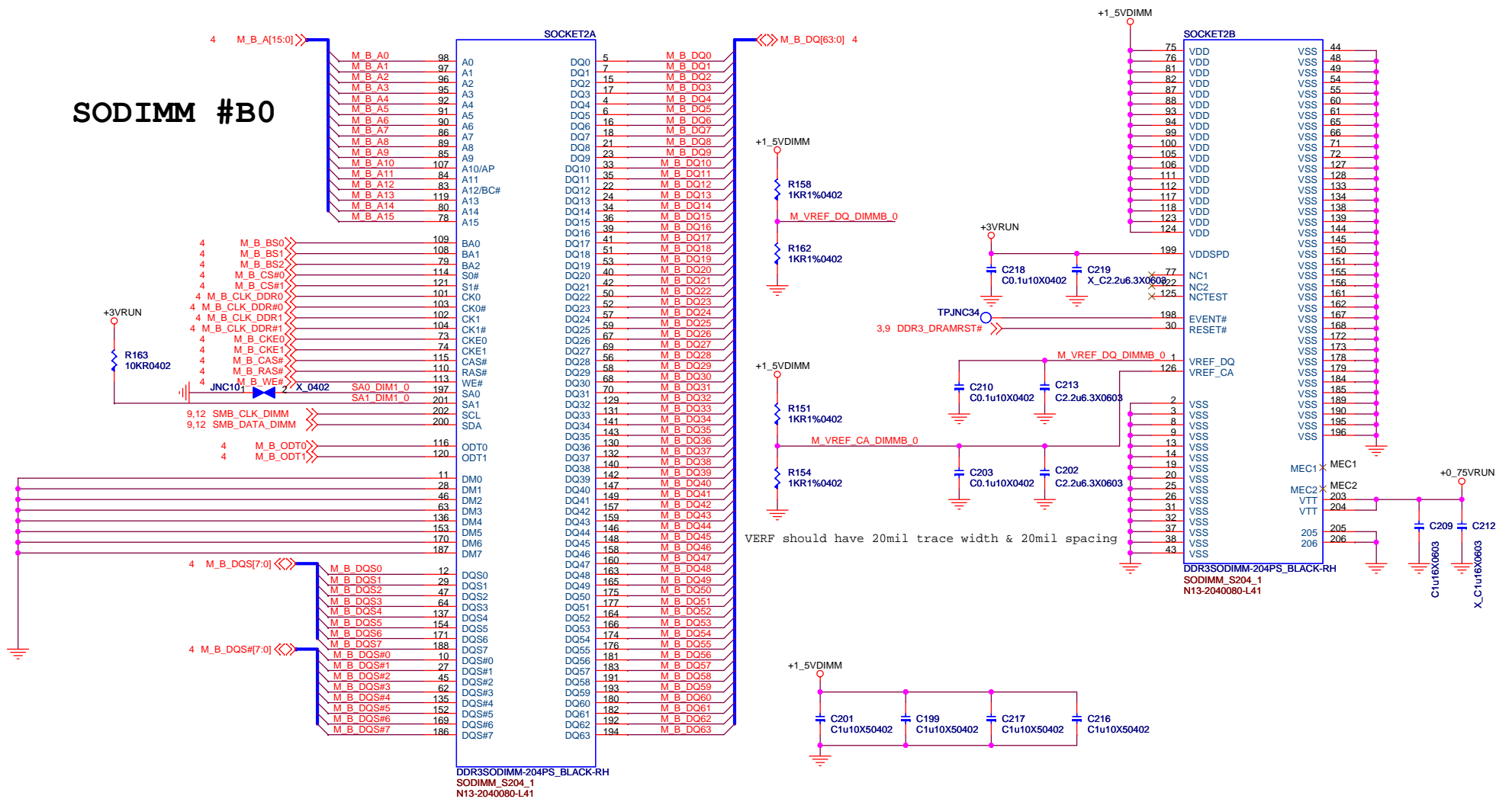
DDR3SODIMM-204PS_BLACK-RH
SODIMM_S204
N13-2040060-L41



VERF should have 20mil trace width & 20mil spacing

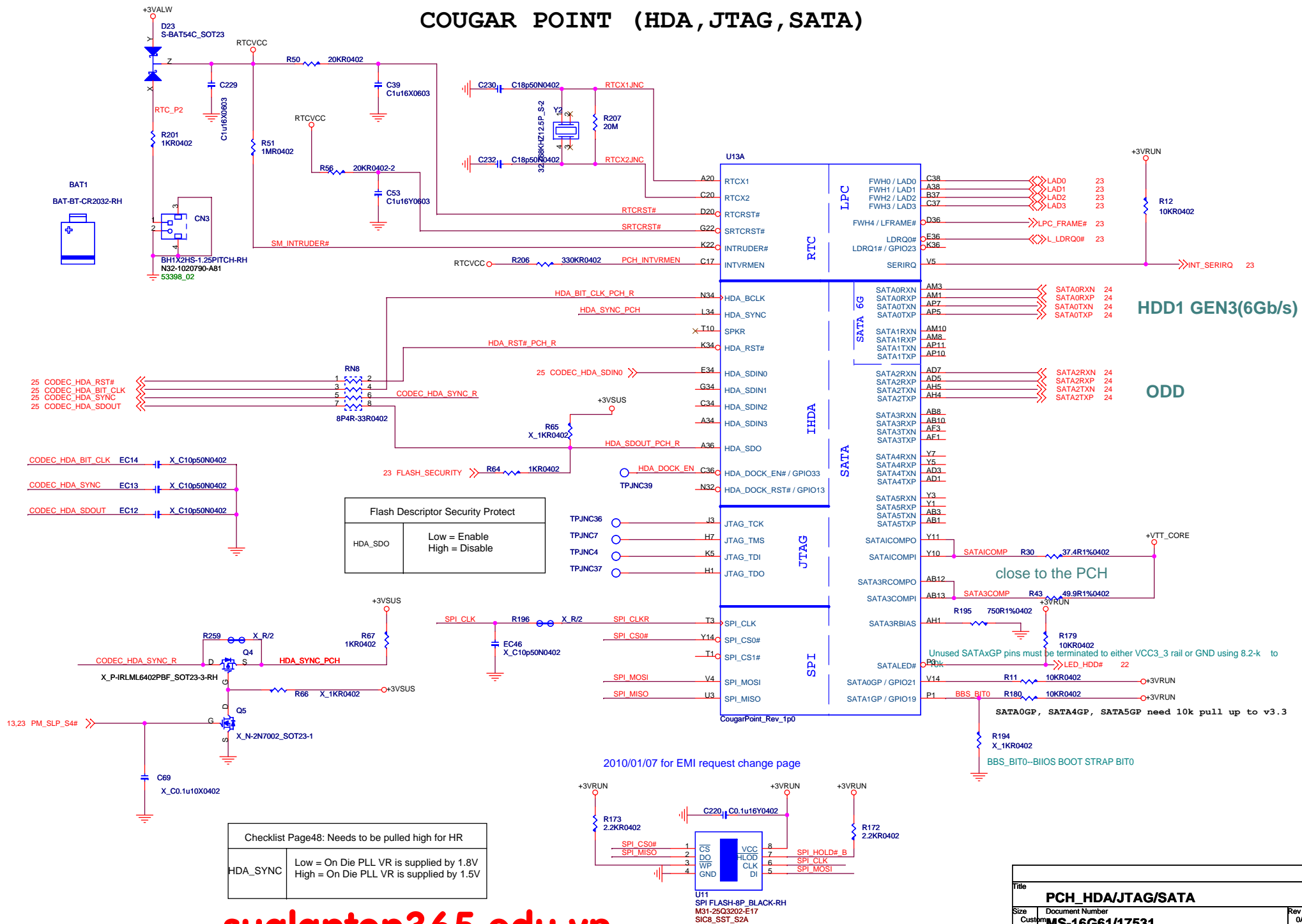
Title				
DDR3 SODIMM A0				
Size	Document Number			Rev
Custom	MS-16G61/17531			0A
Date:	Wednesday, September 29, 2010	Sheet	9	of 42

SODIMM #B0

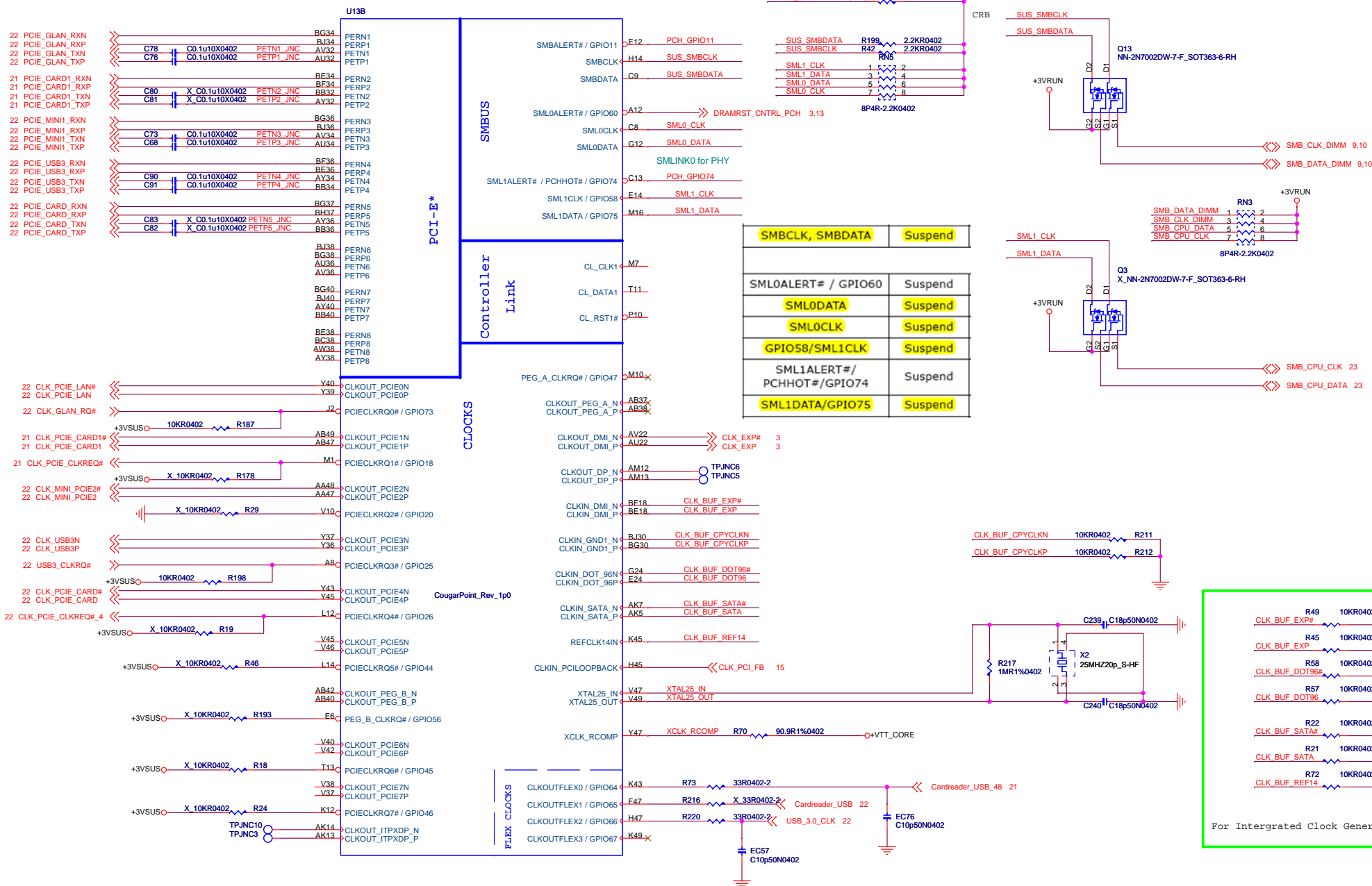


Title			
DDR3 SODIMM B0			
Size	Document Number		Rev 0A
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COUGAR POINT (HDA, JTAG, SATA)



COUGAR POINT (PCI-E, SMBUS, CLK)



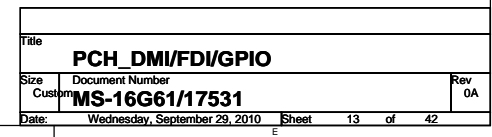
NOTE: If CLKREQ# control is not needed, say for a free running clock, do not pull-down signal to GND. This will increase leakage in Sx states. A 10 kOhms±5% external pull-up resistor still needs to be used, but the corresponding CLKREQ# function can be disabled via Intel® Management Engine (Intel® ME) FW. Please refer to Intel ME FW Bring Up Guide for configuring/disabling CLKREQ#.

Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

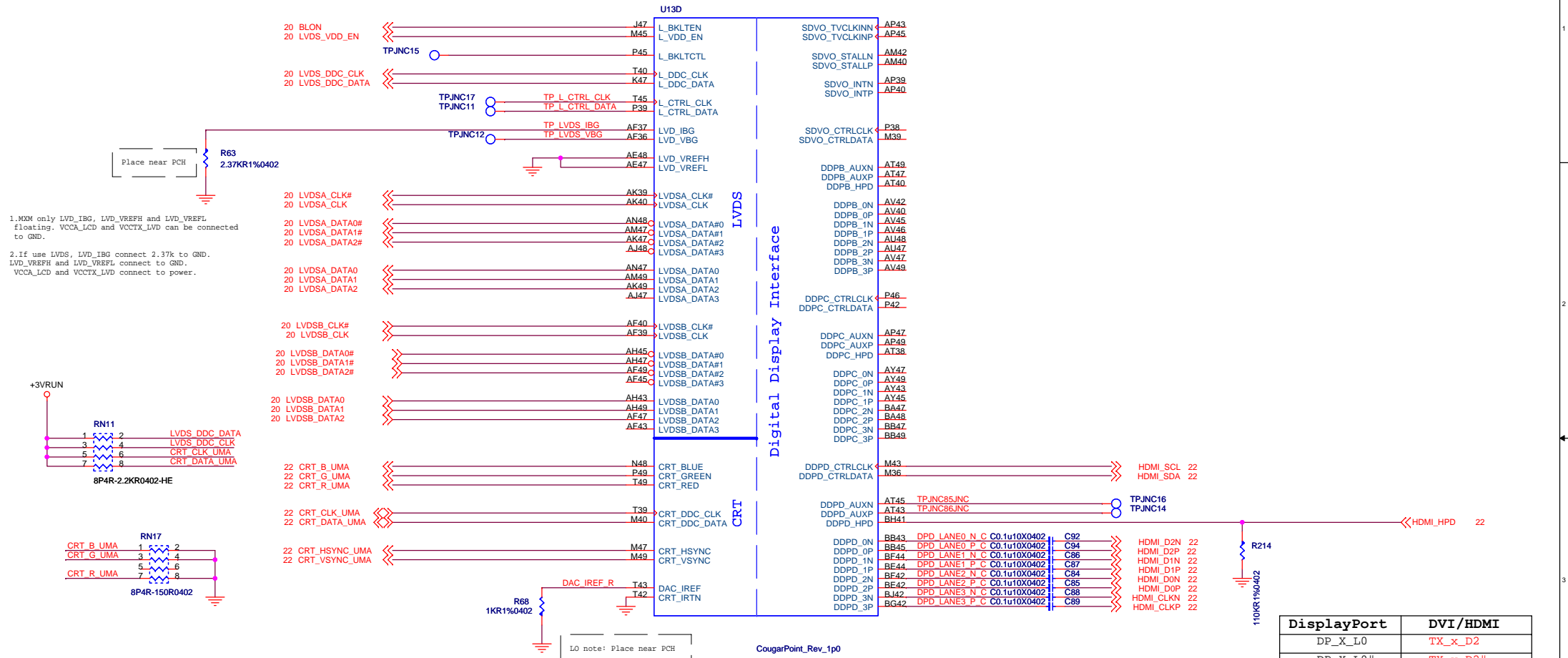
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Title				
PCH_PCIE/SMBUS/CLK				
Size	Document Number			Rev
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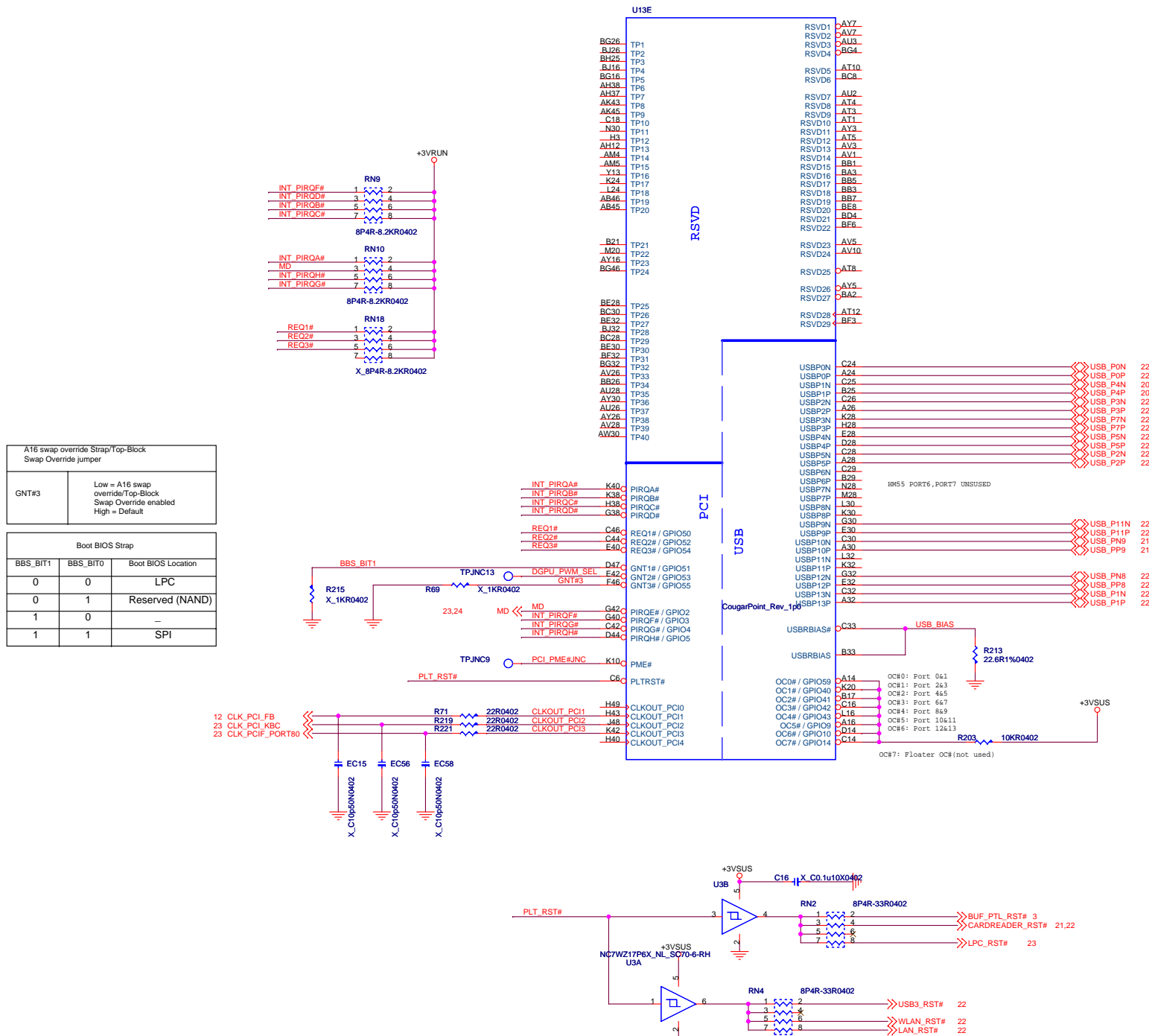


COUGAR POINT (LVDS,DDI)



DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

COUGAR POINT (PCI,USB,NVRAM)



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Title	PCH_PCI/USB/NVRAM		
Size	Document Number	Rev 0A	
Customer	MS-16G61/17531		
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GPIO0 & 6 & 16 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN
GPIO57 --If not used,require pull up 3VSUS
GPIO15--High is support TLS,internal pull-down
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin
GPIO35 --Un- Muxed. If not used Can be NC

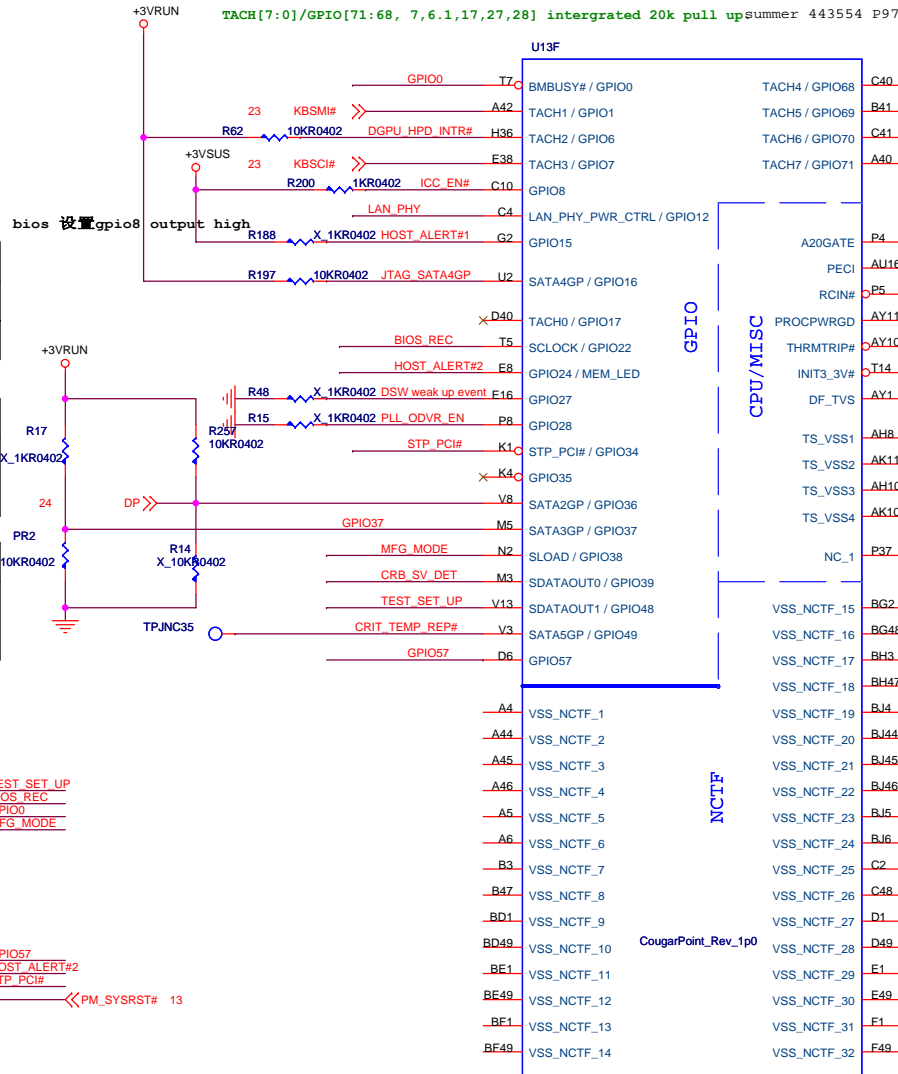
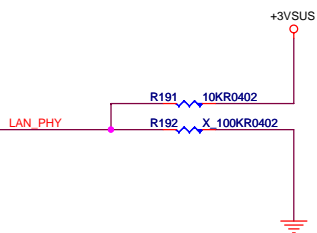
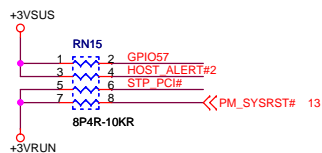
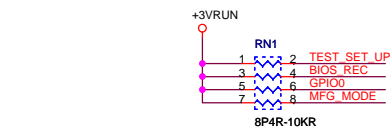
COUGAR POINT (GPIO,VSS_NCTF,RSVD)

GPIO8 is no longer needed as a functional strap for Integrated clocking. Integrated Clock Enable functionality is achieved via soft-strap. The current default is Clock Enabled.

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable) Low: Disable

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same voltage (DC coupling mode)default

FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same voltage (DC coupling mode)default



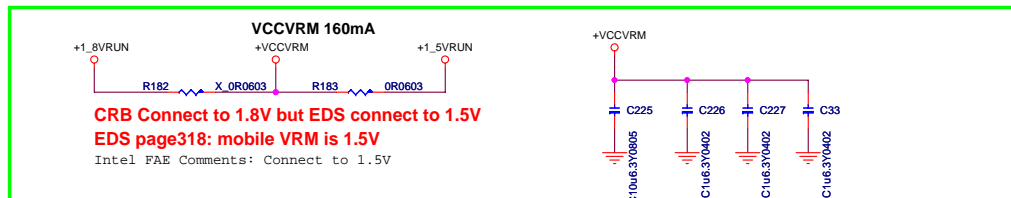
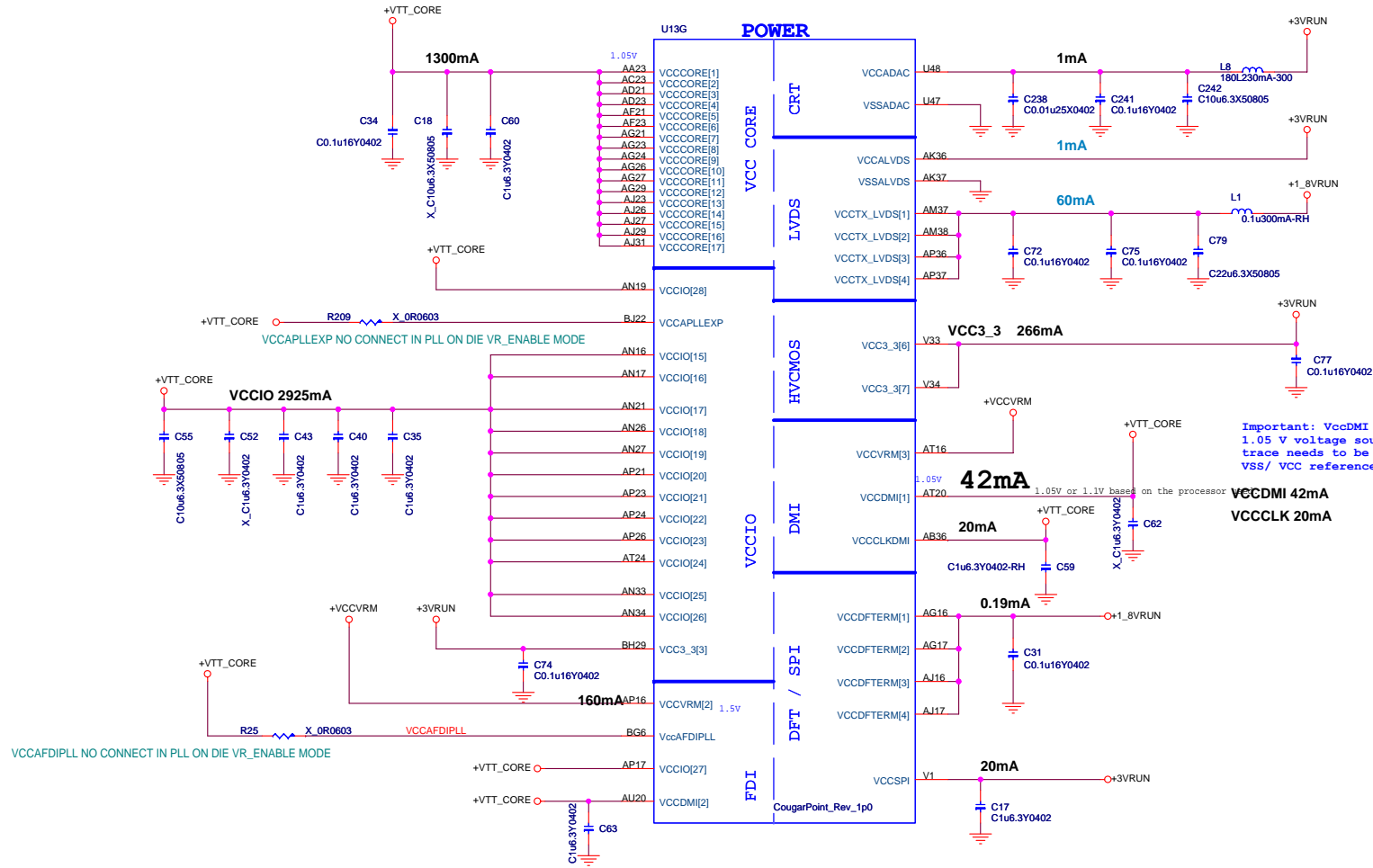
intergrated 20k pull up.

DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW Set to VCC when High

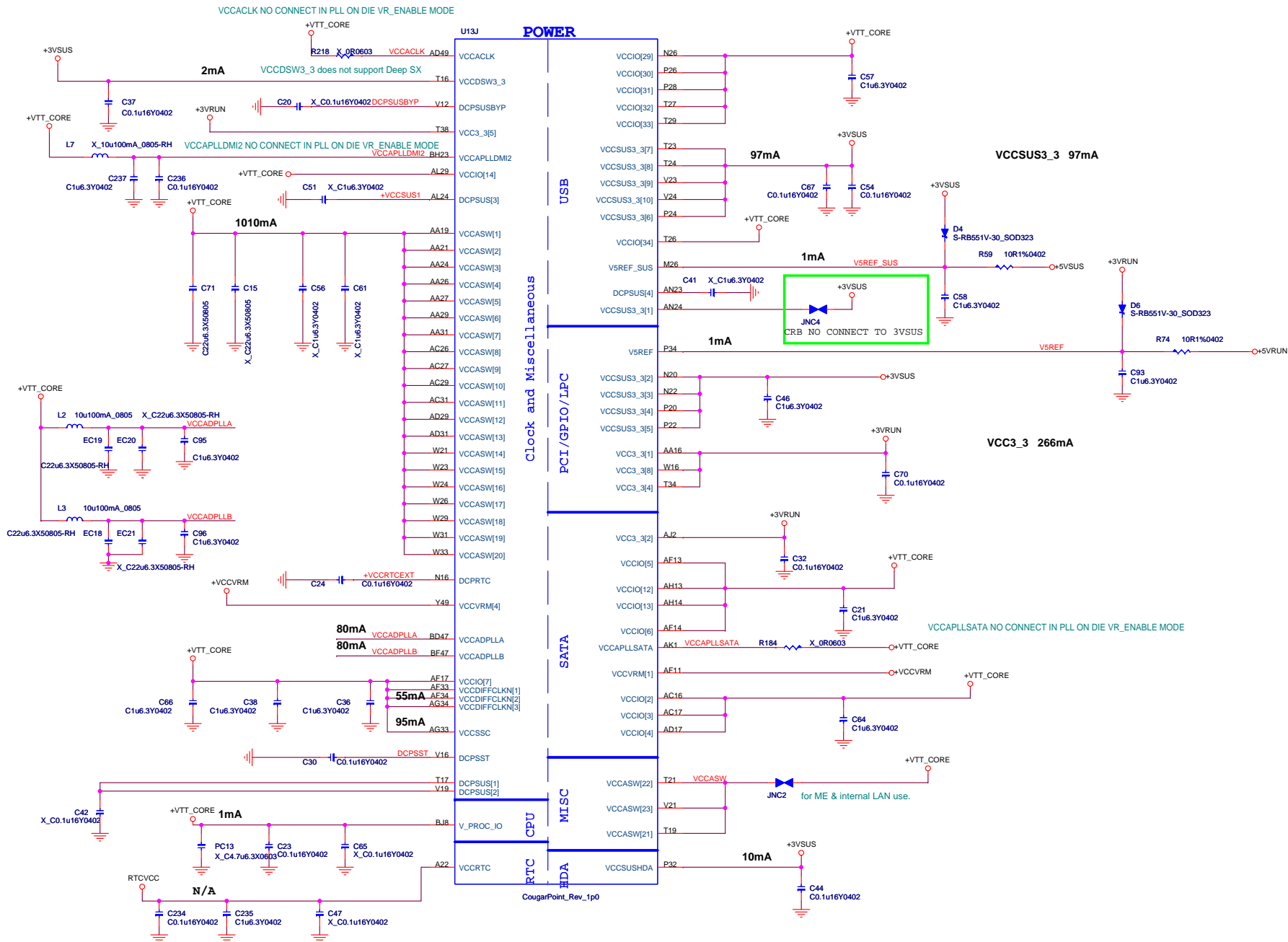
Intel Comments:
Reserve 0 ohm option in these pins
pins AH8, AK11, AH10 & AK10) to GND.
These signals should not float on the motherboard. They should be tied to GND directly.

CRB_SV_DET	
GPIO39	High: External GFX Low: Internal GFX

COUGAR POINT (POWER)

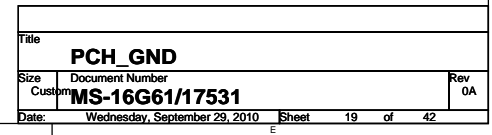


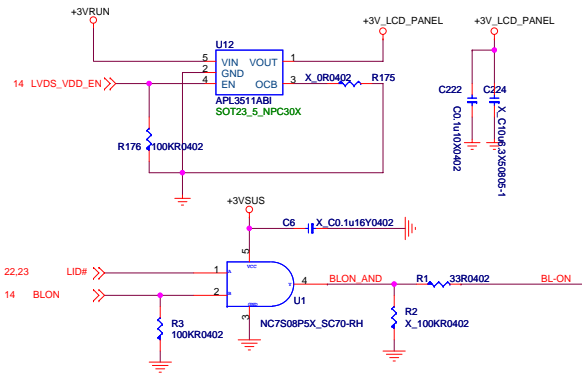
COUGAR POINT (POWER)



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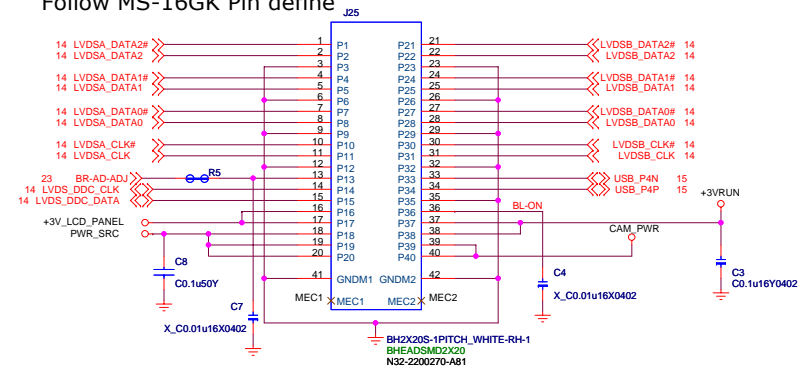




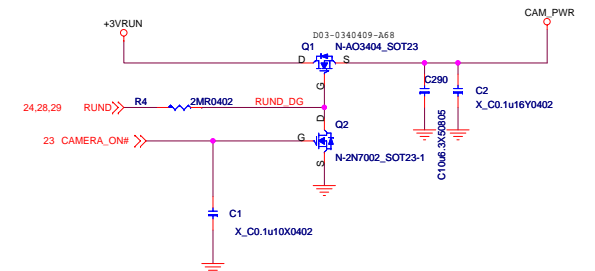
ChA.L

Follow MS-16GK Pin define

ChB.H

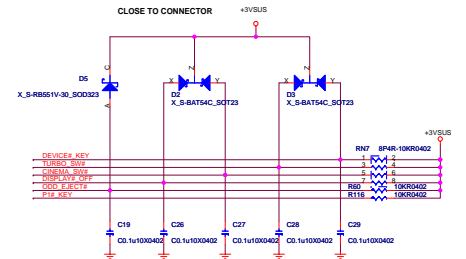
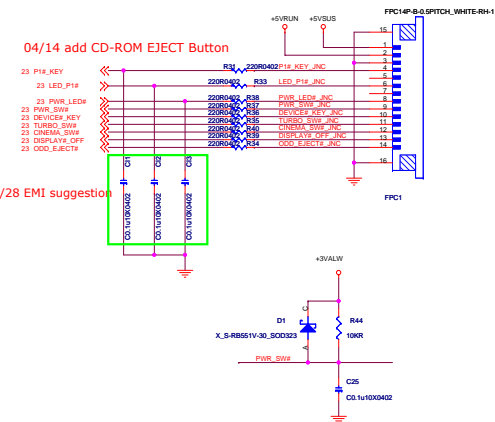
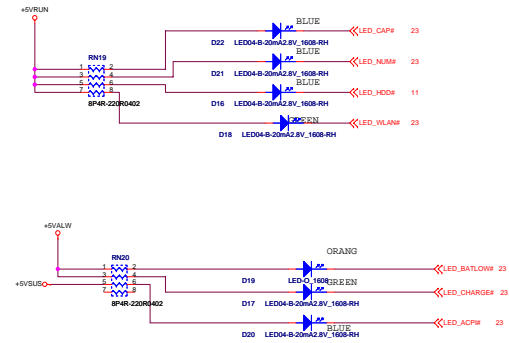
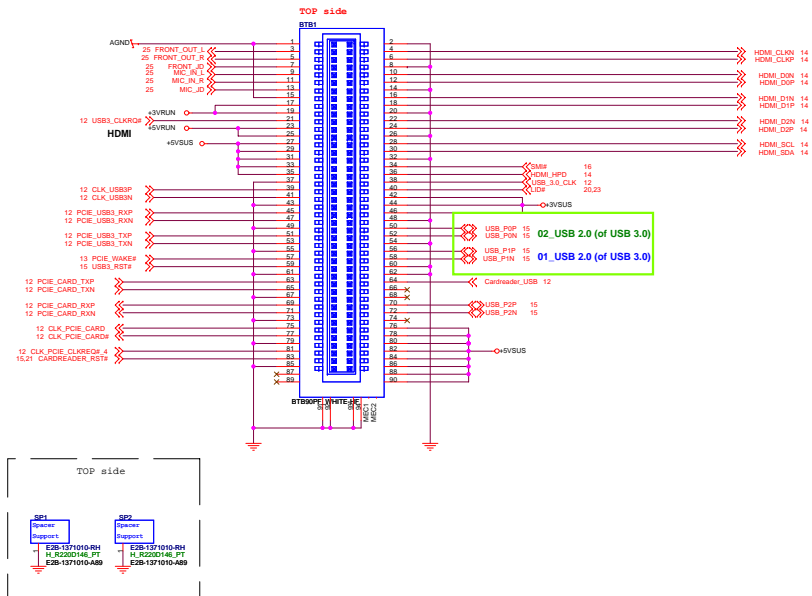


CAMERA LVDS ON

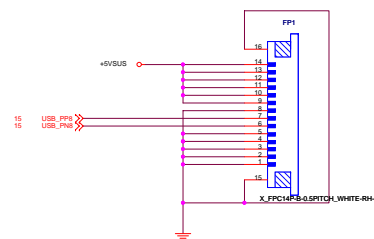
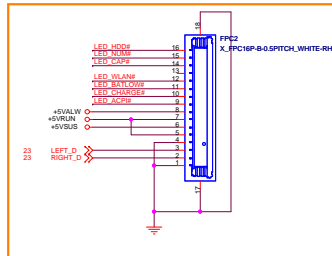


Title			
CRT/LVDS/CCD			
Size	Document Number	Rev	
Custom	MS-16G61/17531	0A	
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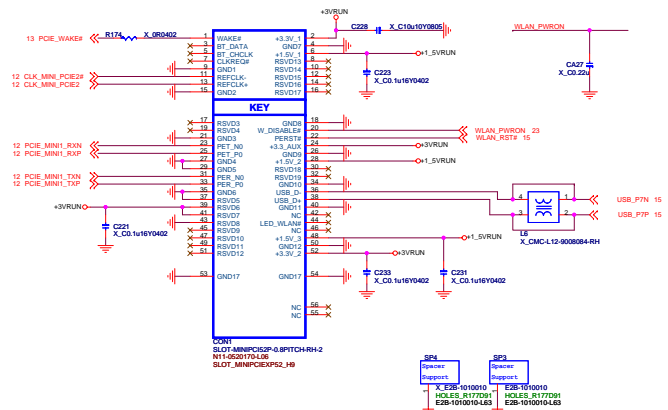
LED



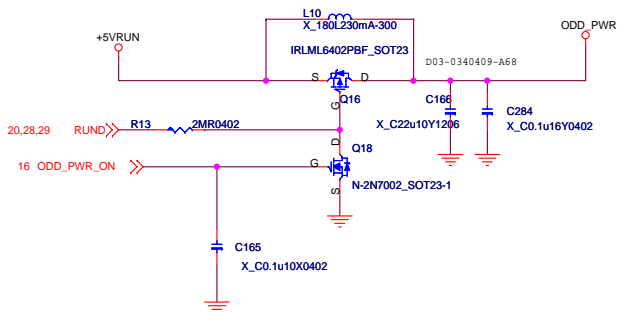
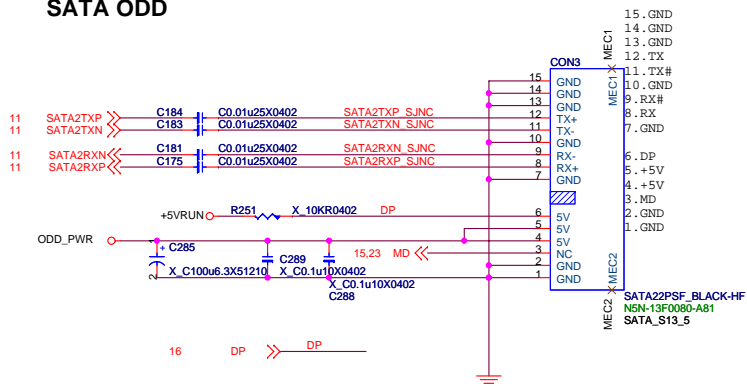
04/06 Modify 16Pin CONN. P.53



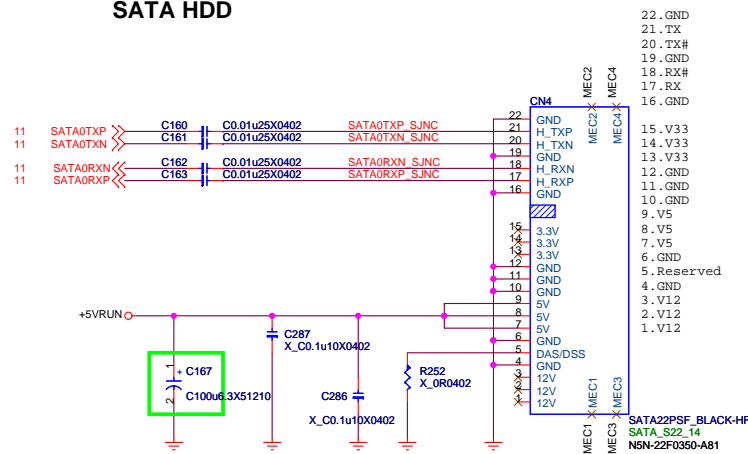
WLAN



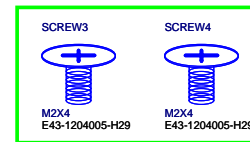
SATA ODD



SATA HDD

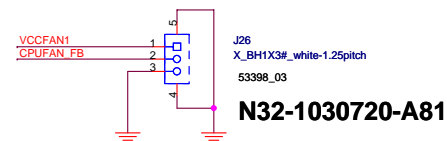
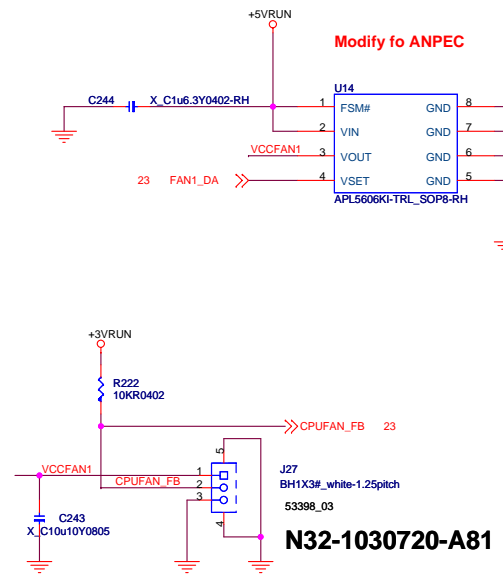


2009/05/15 for Staggered Spin-up 华硕币

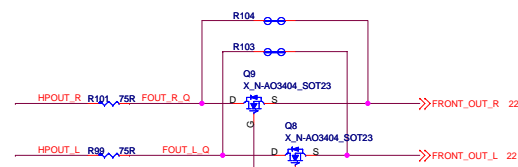
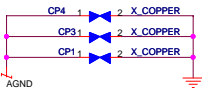
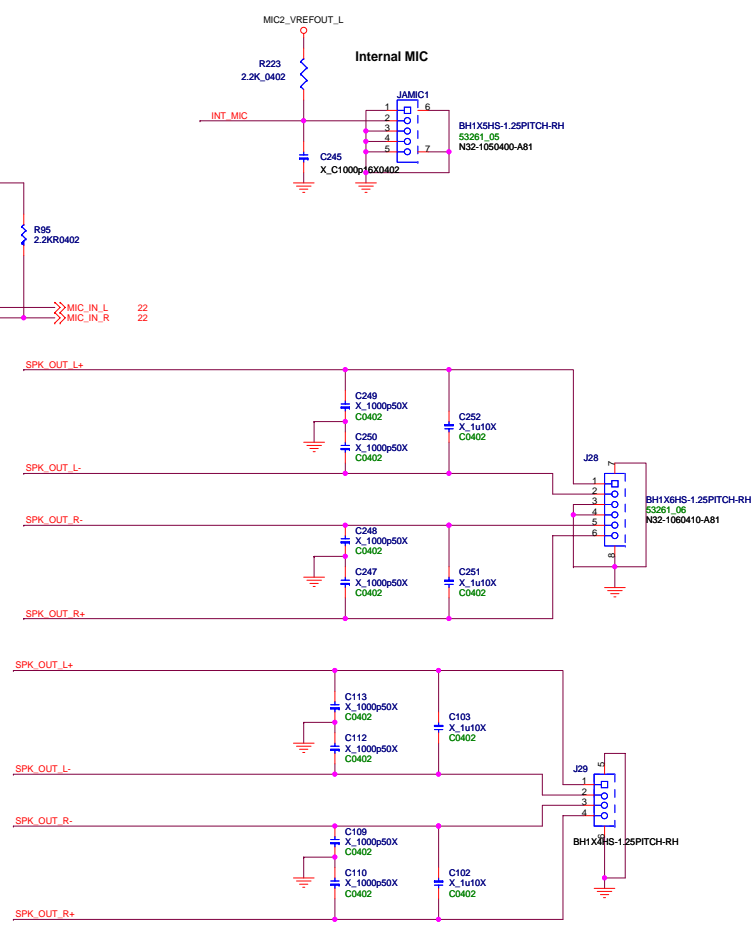
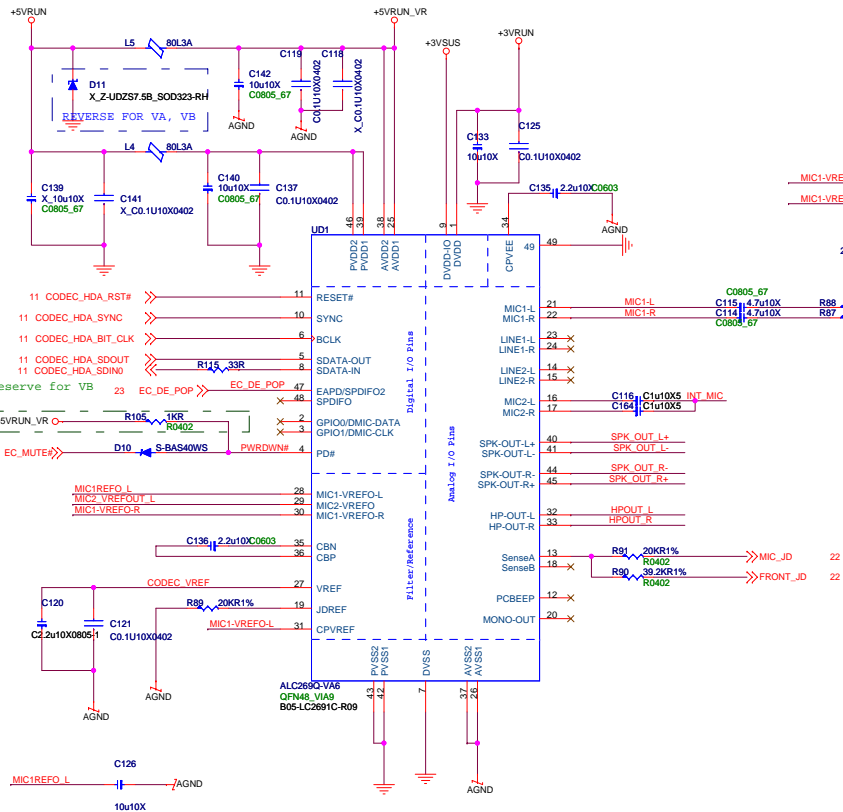


03/30 Add SCREW3, SCREW4 for ME request

CPU FAN

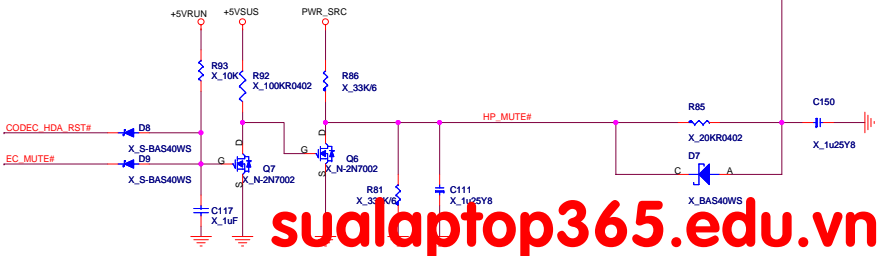


MSI MICRO-STAR INT'L CO.,LTD.			
Title			
HDD2/ODD/ESATA Combo/FAN/BT			
Size	Document Number	Rev	
Customer	MS-16G61/17531	0A	
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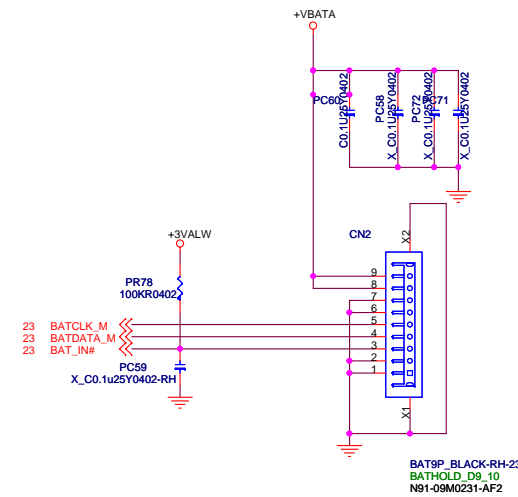
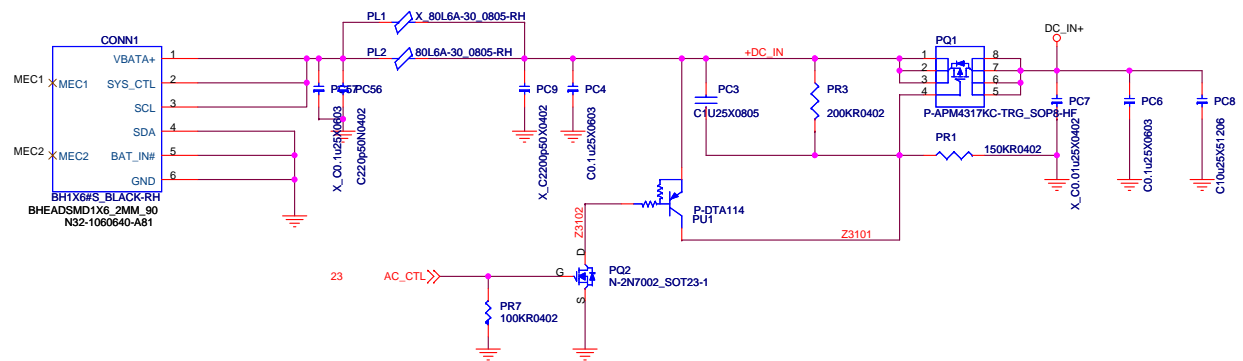


Speaker wire length is less than 20cm

20 mil trace width is required for 4ohm loading
10 mil trace width is required for 8ohm loading
the trace length/ Speaker wire length of SPKL+/L-/R+/R- is same as possible as you can.

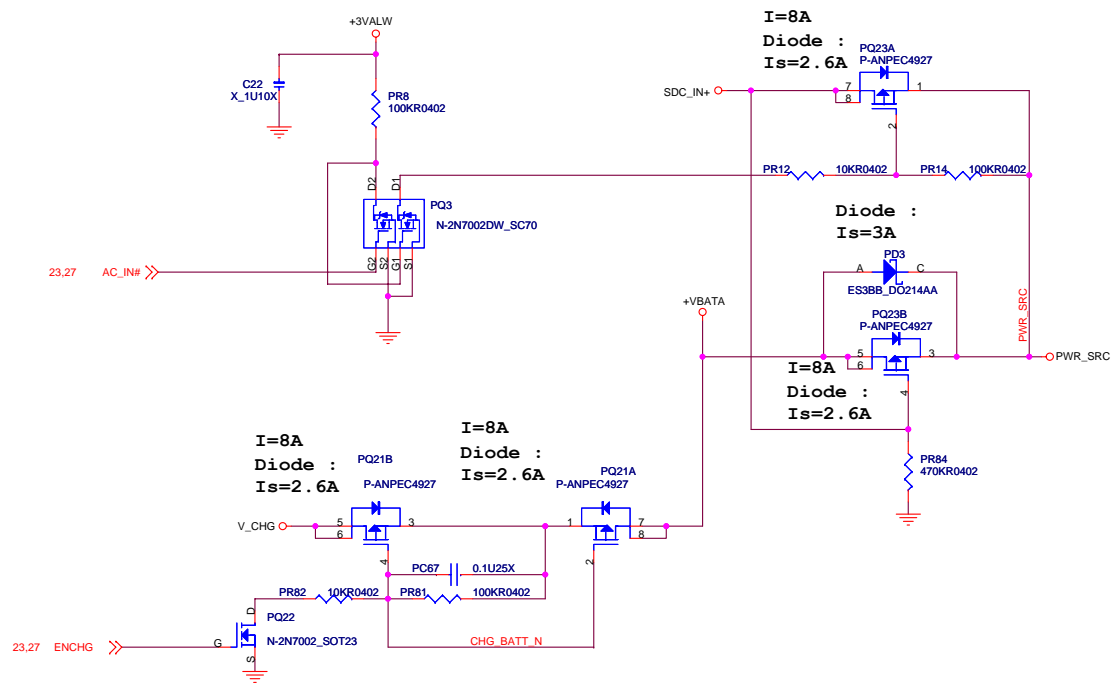


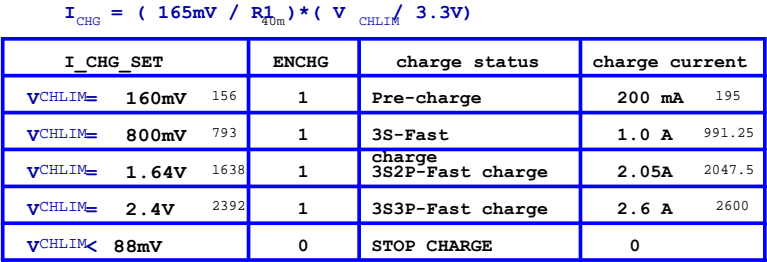
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JBAT1 Pin Definition

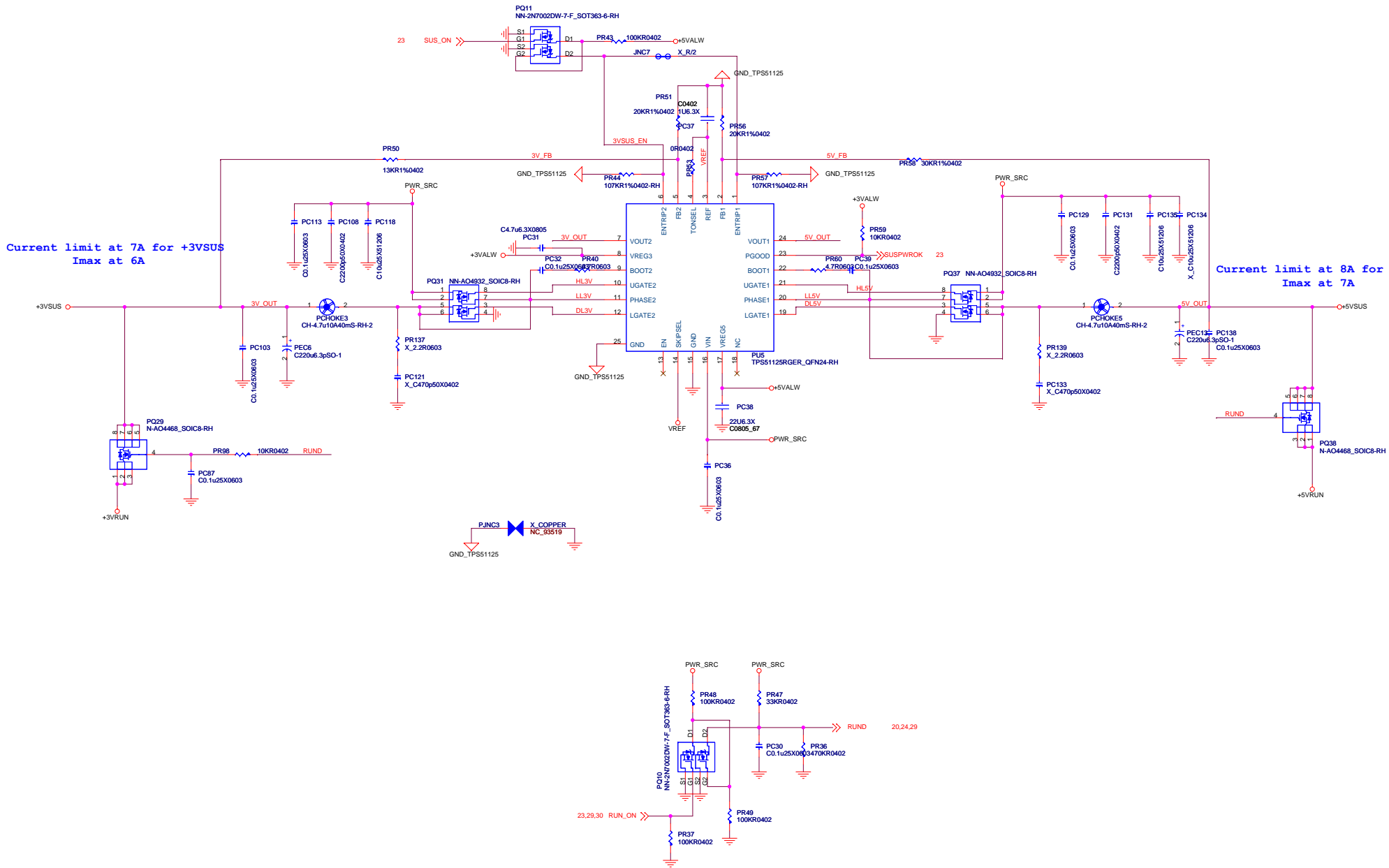
- 1: GND
- 2: GND
- 3: BAT_IN#
- 4: SMBDATA
- 5: SMBCLK
- 6: NC
- 7: NC
- 8: VBATA+
- 9: VBATA+

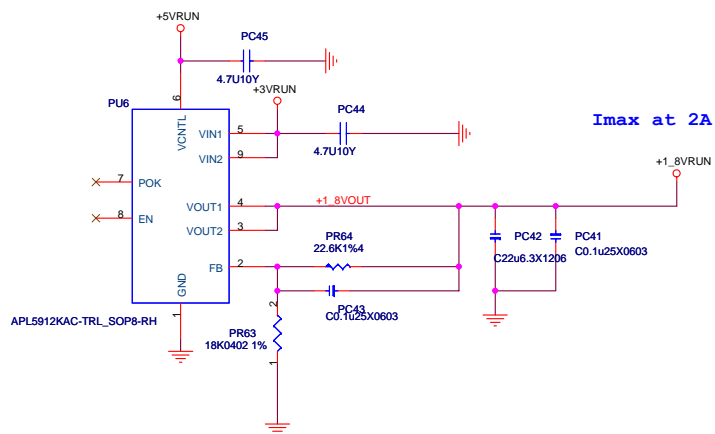
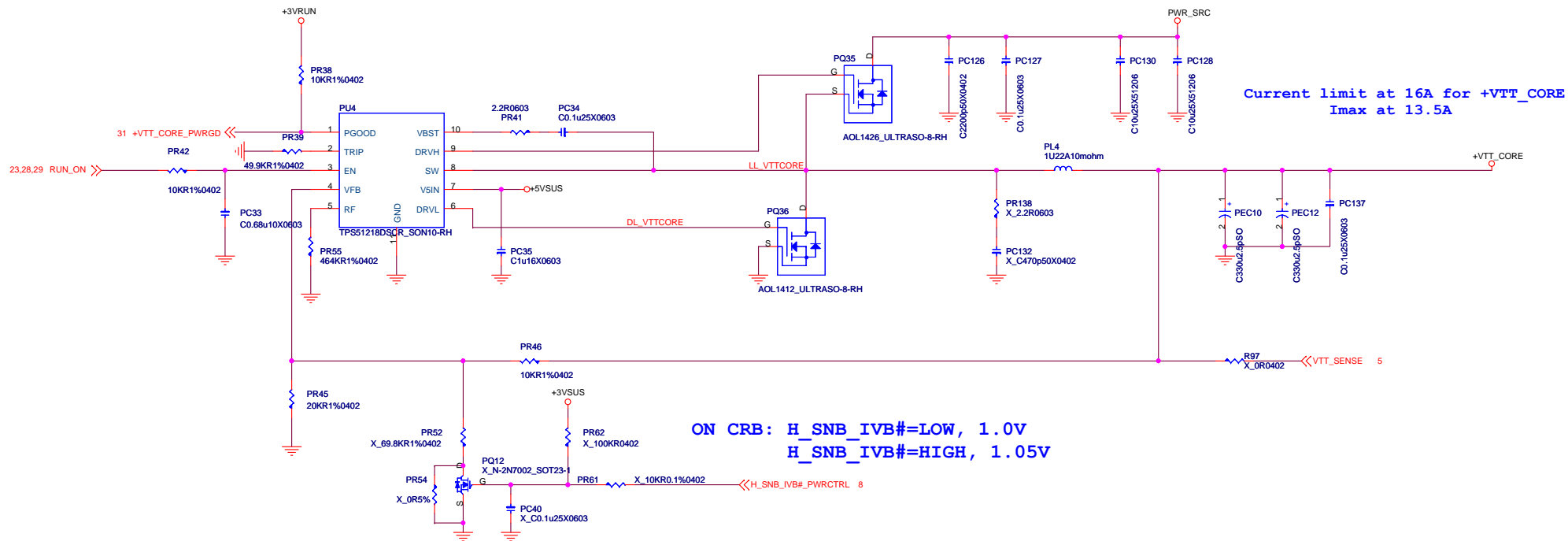


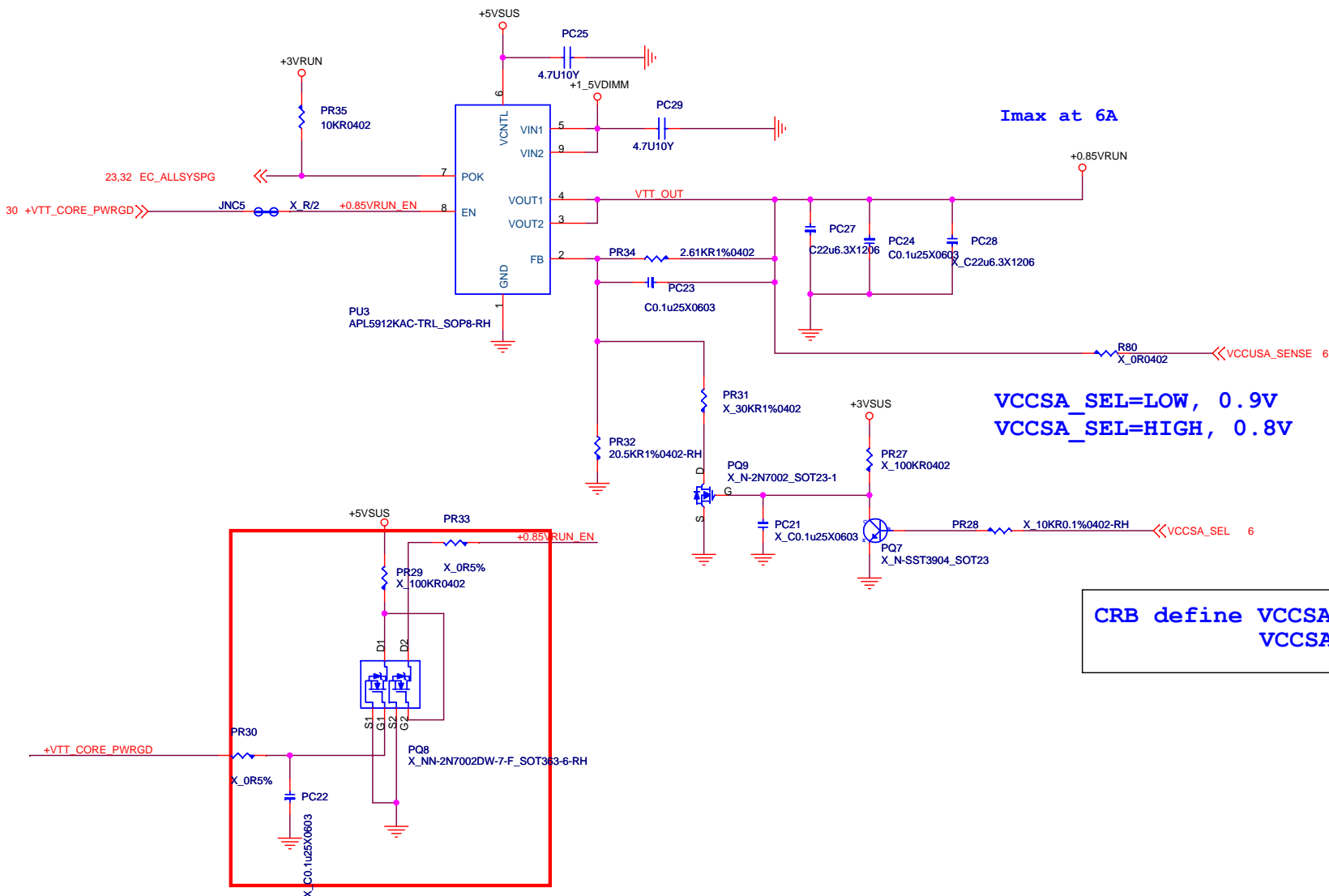


Current limit at 7A for +3VSUS
Imax at 6A

Current limit at 8A for +5VSUS
Imax at 7A

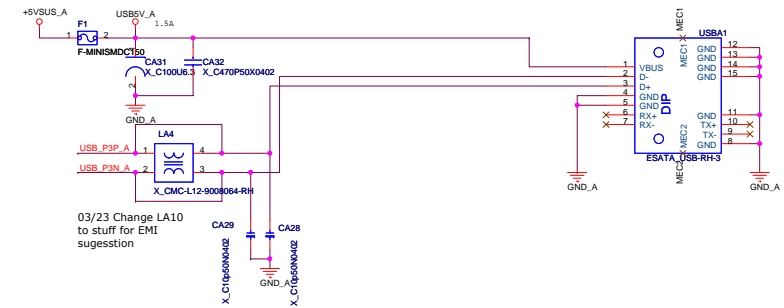
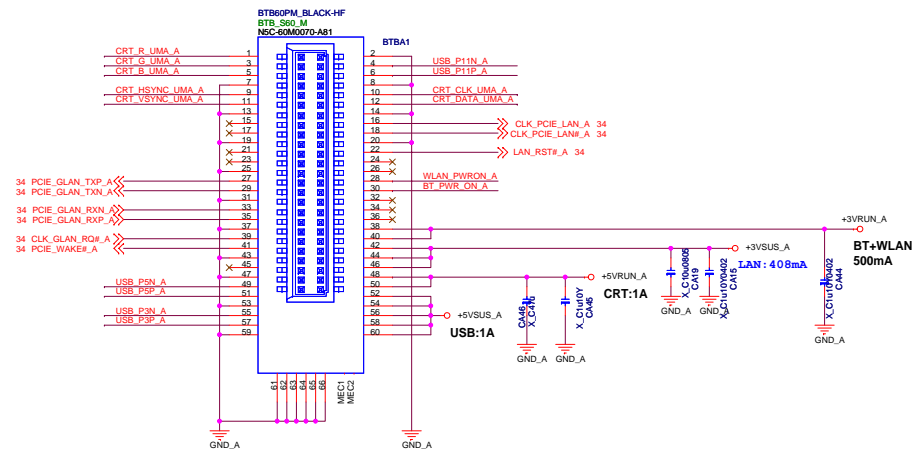






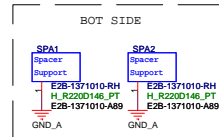
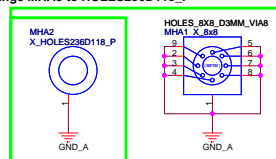
Title		
0.85V		
Size	Document Number	Rev
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(㉔ESATA,USB,LAN,CRT,BT+WLAN)



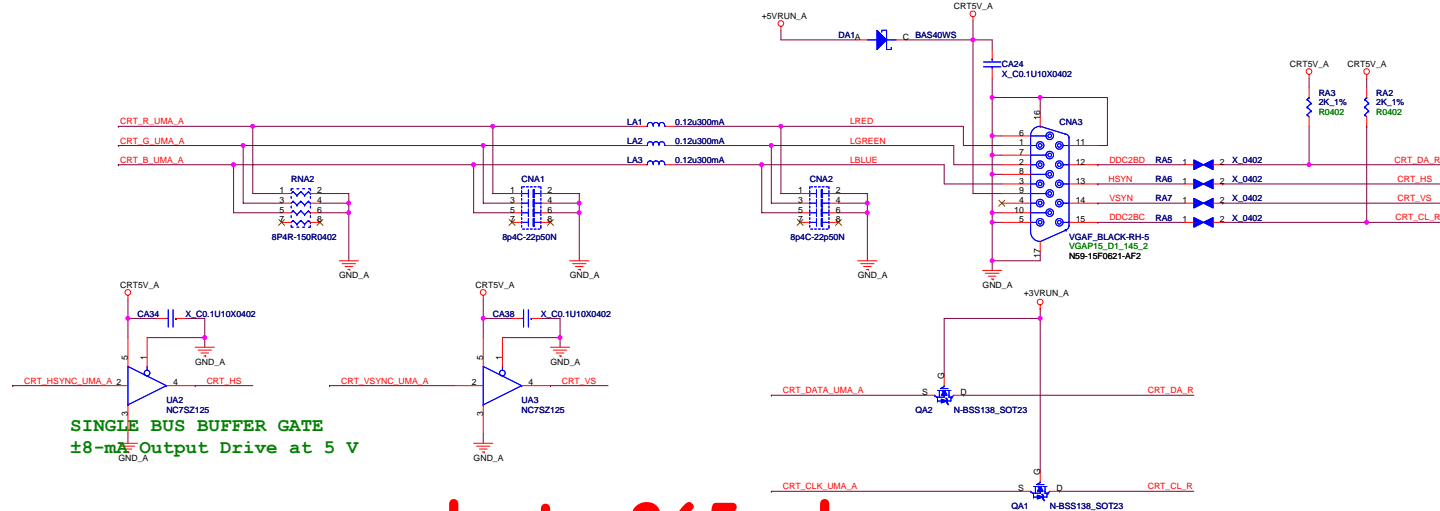
02/25 Change MHA8 to HOLES_R276D185P_PT

03/30 Change MHA8 to HOLES236D118_P

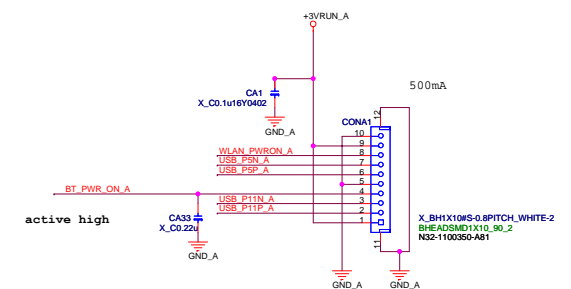


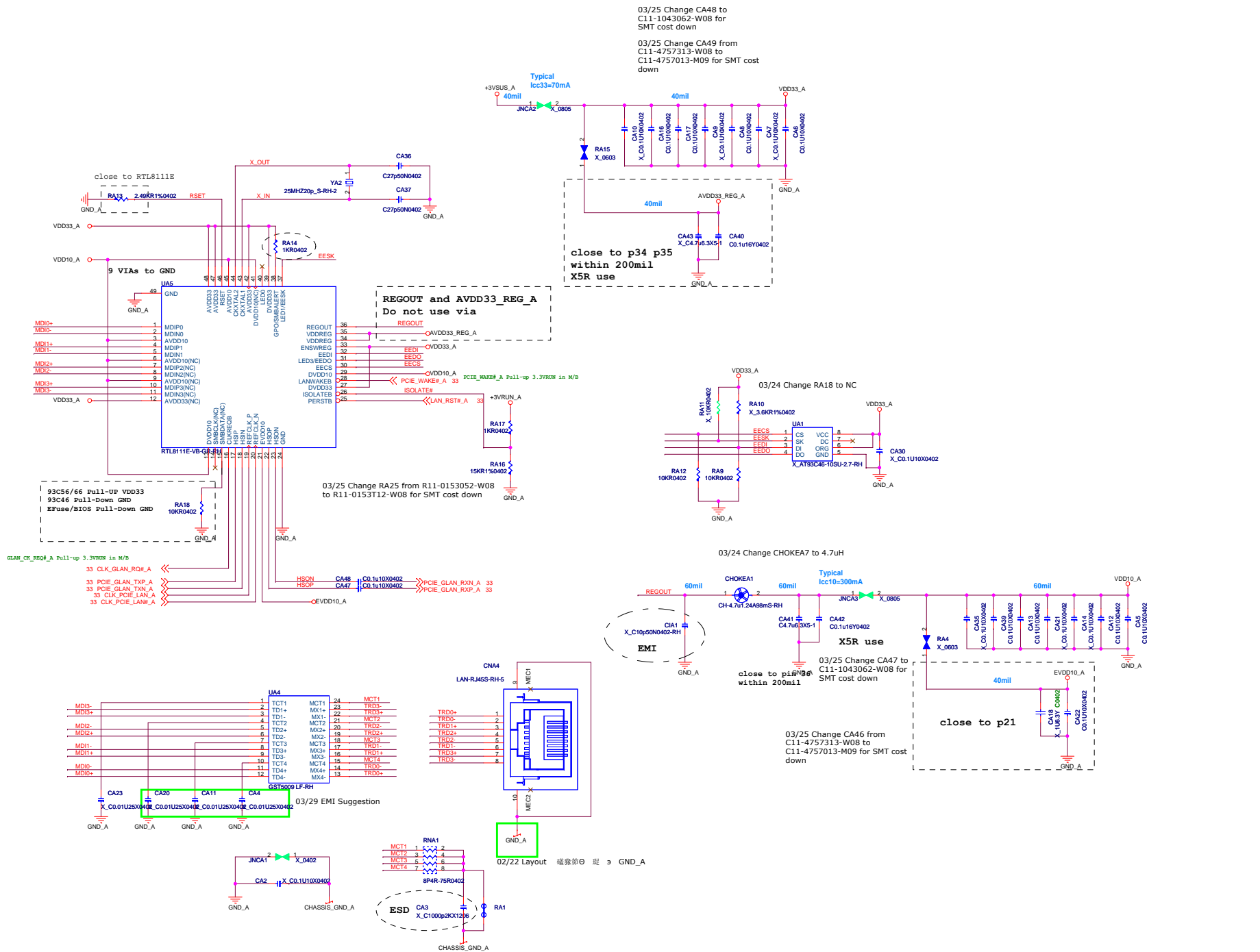
02/23 Change to 8 vias for EMI sugesstion

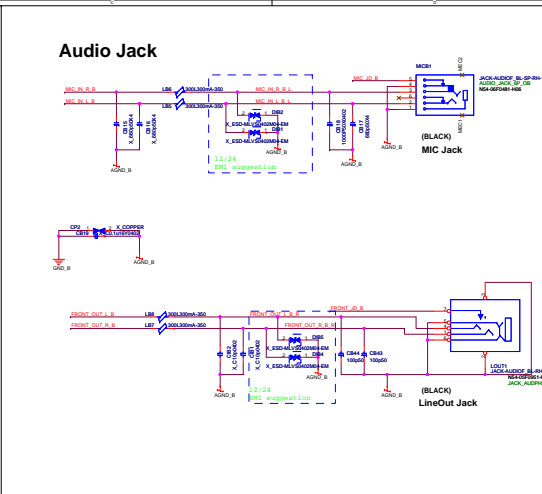
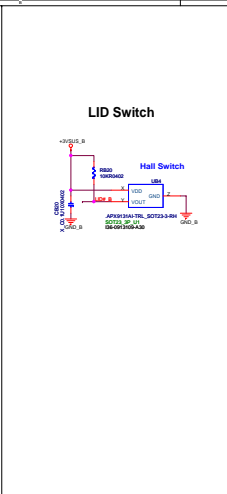
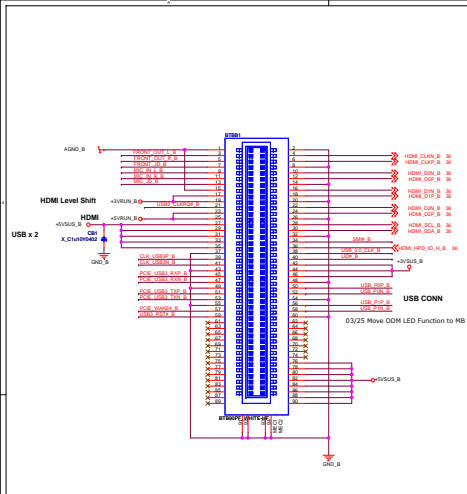
D-Sub Connector



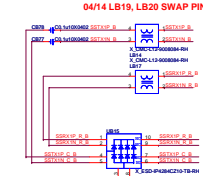
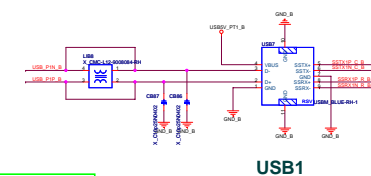
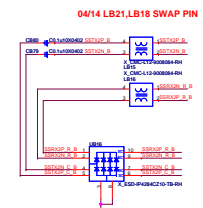
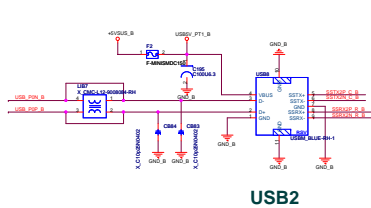
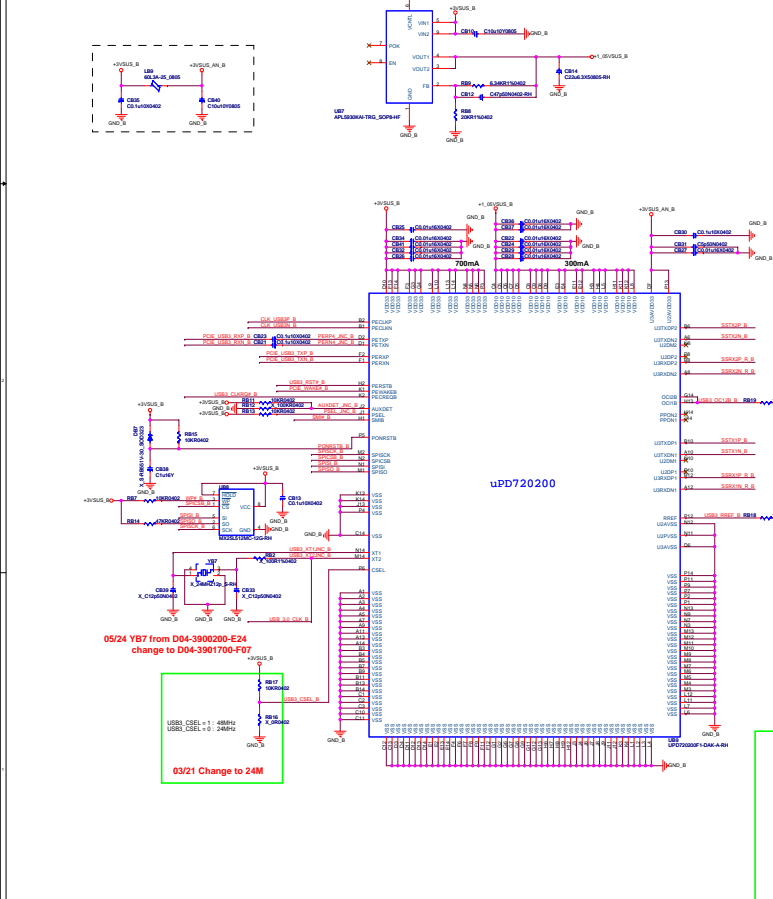
BT and WLAN Combo Connector



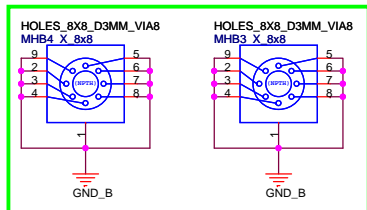
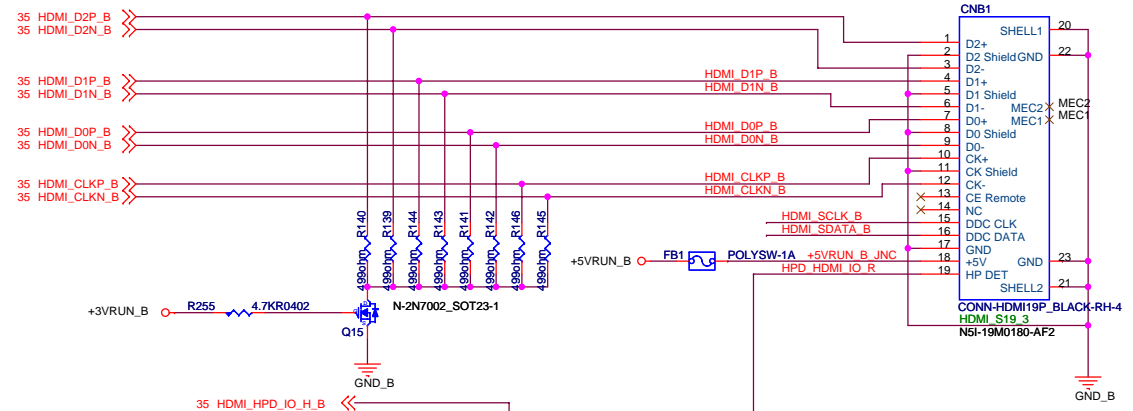




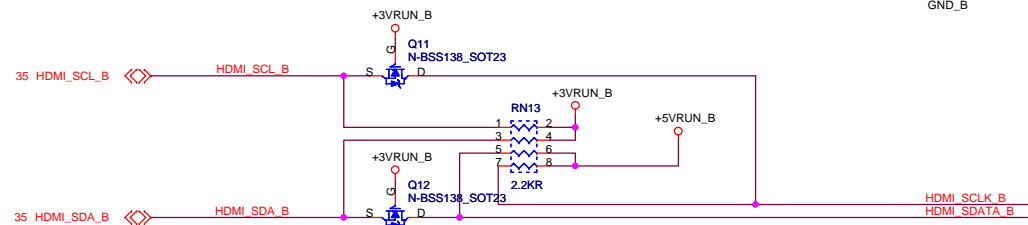
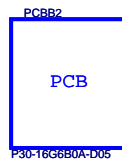
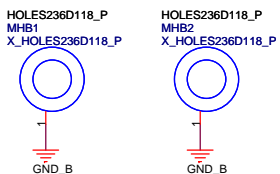
(Card reader, USB 3.0 x 2)
USB 3.0 Connector



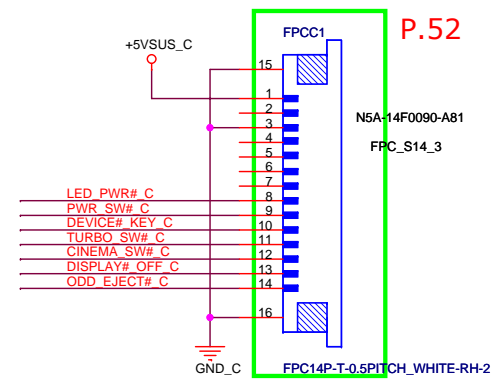
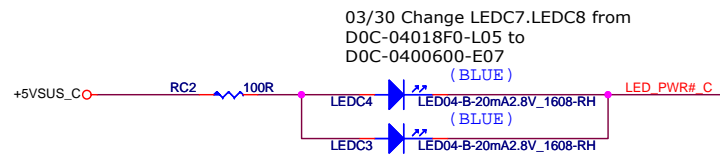
HDMI Connector



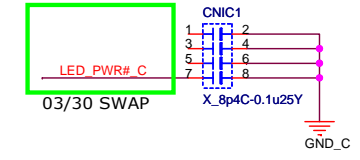
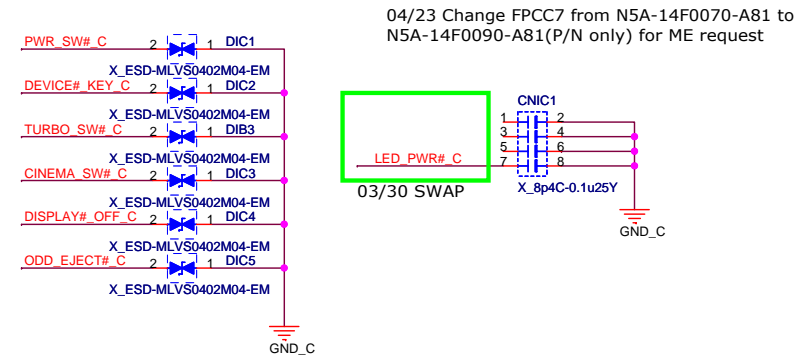
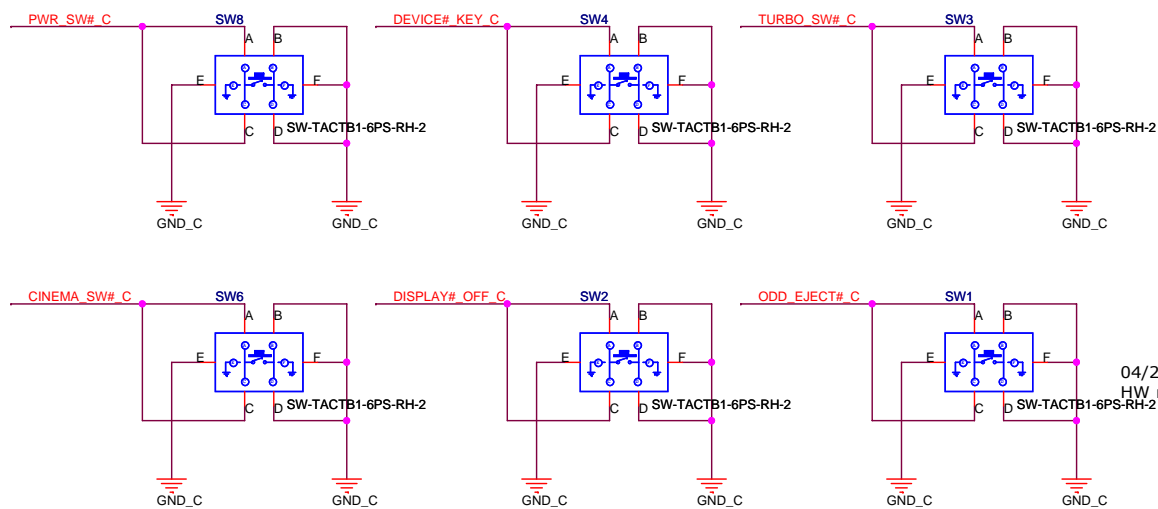
02/23 Change to 8 vias for EMI sugesstion



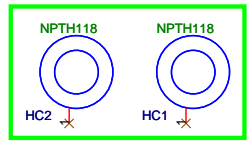
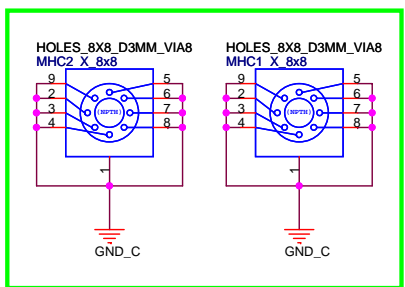
MSI MICRO-STAR INT'L CO.,LTD.			
Title			
Audio/USB*2/Conn			
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03/29 Remove ECO and Cinema LED for ID request




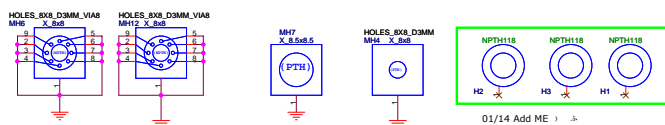
04/28 Fix SWC8's HW mismatch



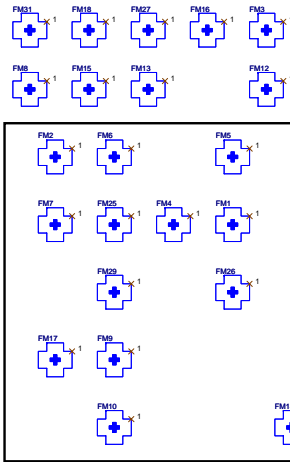
03/26 Add ME



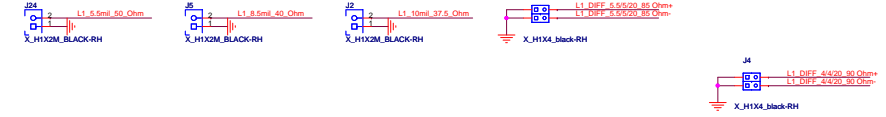
 MSI <small>Micro-Star International Co., Ltd.</small>		MICRO-STAR INT'L CO.,LTD.	
Title			
PWR SW / LED			
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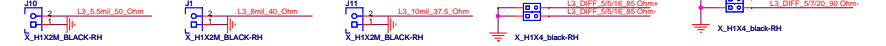
01/14 Add ME



TOP



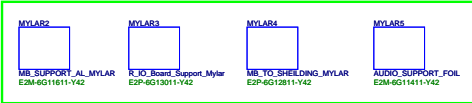
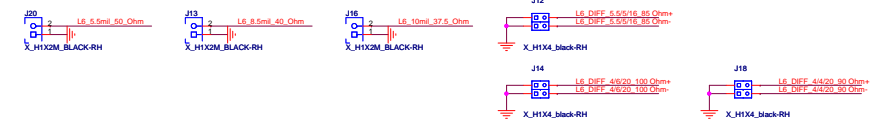
INT3



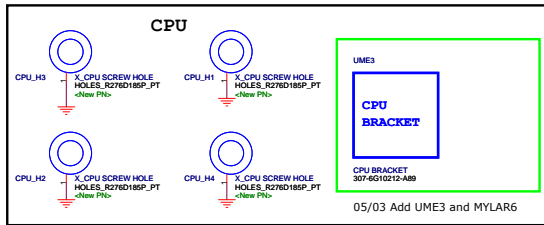
INT4



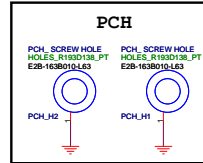
BOTTOM



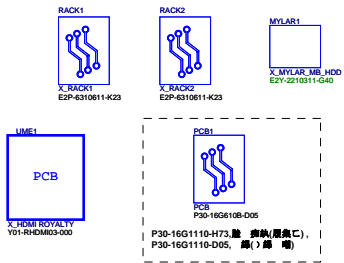
04/23 Add MYLAR2,MYLAR3,MYLAR4,MYLAR5 for ME request



03/04 Change CPU Holes to NC

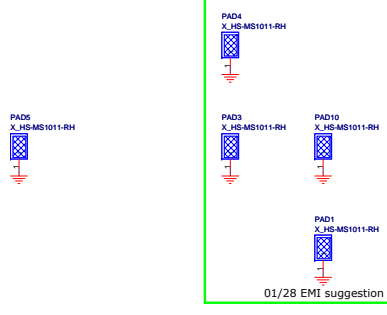


05/03 Add UME3 and MYLAR6

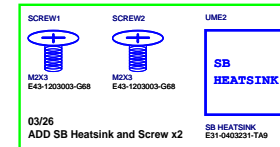


TOP SPRING

BOT SPRING

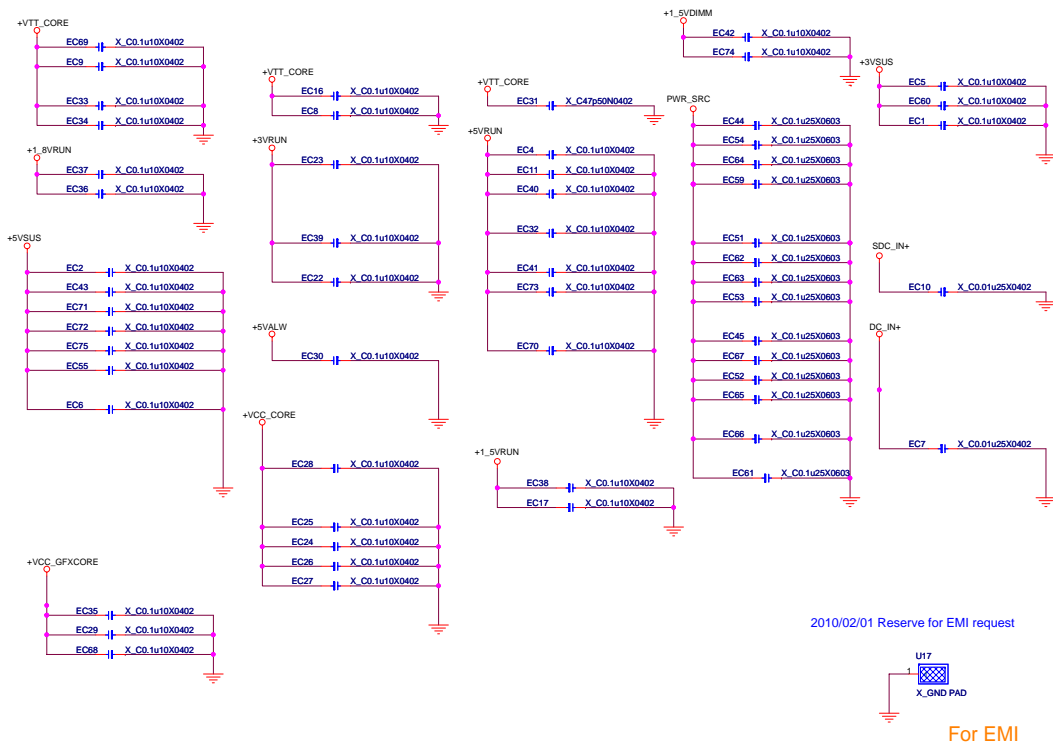


01/28 EMI suggestion



03/26 ADD SB Heatsink and Screw x2

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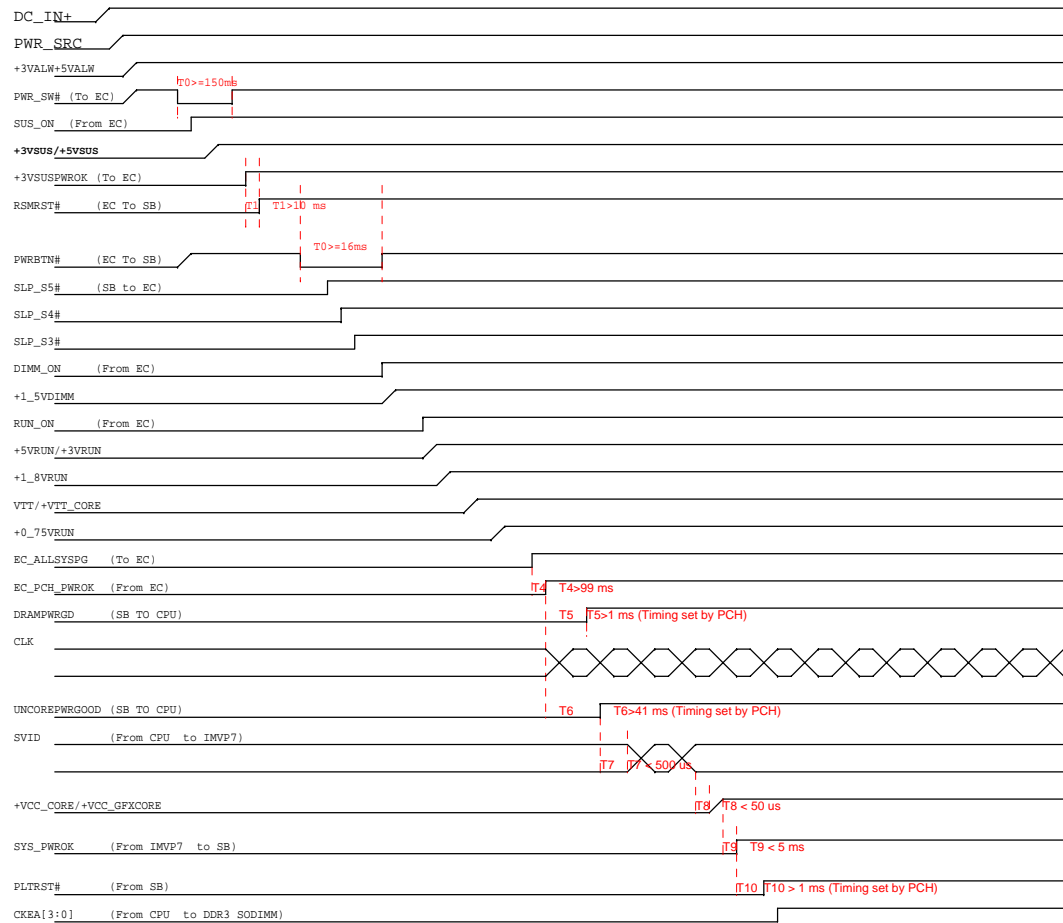


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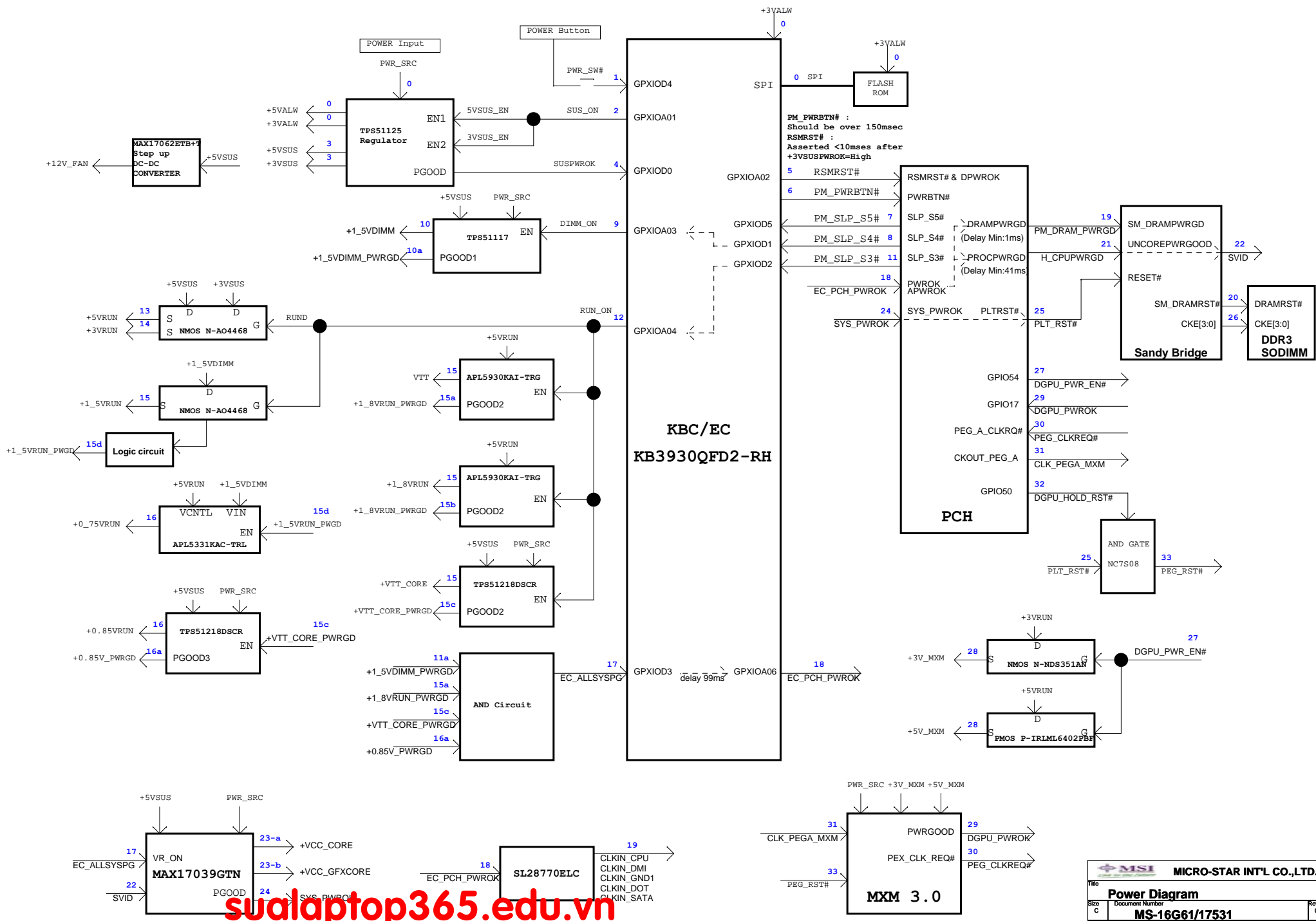
S5-S0

EC programming timing

Intel Huron River timing SPEC



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Power down Sequence DC mode S0 to G3

S0-S5

EC programming timing

Intel Huron River timing SPEC

